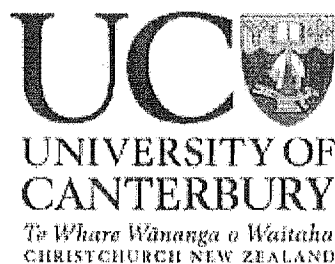

The Development of a Low-Cost Strong Motion Seismograph

A thesis submitted in fulfilment
of the requirements for the degree of
Doctor of Philosophy in Civil Engineering

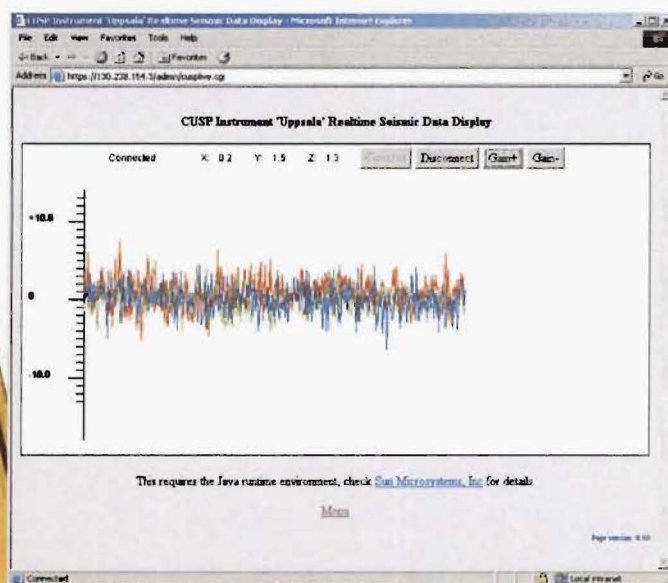
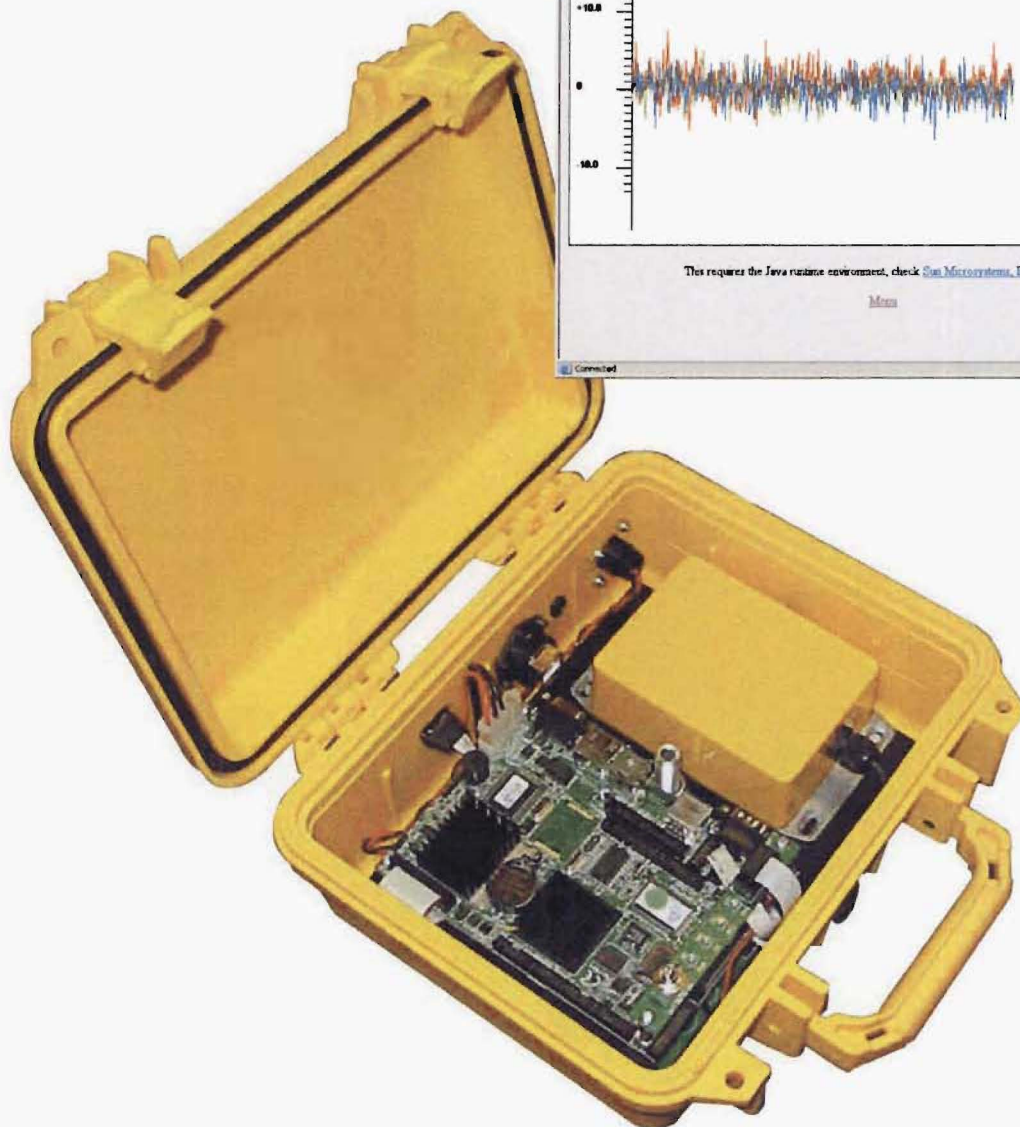
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10 March 2005

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Abstract

This thesis outlines the development of a universal network-based datalogger hardware system, seismic specific sensors and a suite of software to result in a low-cost accelerograph. The primary objective of the research has been to create a product that provides a service lifetime exceeding the 'mean time before failure' of the design's components while still maintaining low construction and maintenance costs. In place of the traditional approach of combining highly-integrated customised circuitry with a custom operating system, the accelerograph has been developed by focusing the design effort at a higher-level system of 'off the shelf' hardware modules which are connected by standard interfaces, with overall control and buffering of application-specific software provided by a generic operating system. The standard interfaces help ensure an ongoing range of compatible, equivalent (or improved) replacement modules, and the generic operating system ensures that they can be integrated quickly and easily with no modification to application-specific software. This buffering of the design from hardware changes increasing the product's tolerance to future module re-specification. The objective to achieve a low initial build cost necessitated the use of low-cost microelectromechanical (MEMS) silicon accelerometers. The non-ideal characteristics of these sensors resulted in the secondary objective of this research, to evaluate MEMS sensors for seismic monitoring purposes and to attempt to mitigate their non-ideal characteristics.

Keywords: Linux, Real-time operating systems, Accelerograph, Data acquisition, Datalogger, COTS, Obsolescence mitigation

Acknowledgements and Thanks

First, I would like to acknowledge the tireless work and support of my supervisors, Drs John Berrill and Bruce Deam and Professor Mike Dewe. Without them the project would have faltered, if not ground to a stop, at one point or another. It has been a long, and at times frustrating, journey to arrive at this point, and any credit given this thesis belongs equally to them.

I would also like to recognise the major contribution to the project, especially in the area of calibration and testing, by Peter Coursey, of the technical staff at the Civil Engineering Department. Also on the technical staff, I am grateful for the advice and ideas of Richard Newton and Mike Weavers.

I also want to acknowledge the work performed on the axial misalignment section by John Berrill, in the calibration PC application by Peter Coursey, and in the curve fitting algorithms of earlier versions by Caroline François-Holden.

Thanks are due to Drs. Mark Chadwick, Jim Cousins and Ken Gledhill of the Institute of Geological & Nuclear Sciences for their help and support. Also thanks to Dr Ivan Skinner and Dr Jarg Pettinga for their information, advice and encouragement.

Funding for the project has been generously supplied by, and gratefully received from, The Brian Mason Technical Trust, the Christchurch City and Canterbury Regional Councils, the University of Canterbury and the EQC Research Foundation.

Thanks go to Reynir Bödvarsson and Roland Roberts from the Institutionen för geovetenskaper, at the Geophysics department at Uppsala University, Sweden for their hospitality whilst I was an exchange student with them.

For ceaseless encouragement and moral support, I would like to thank my parents, Barry and Jan, plus my siblings, Mathew and Kerry, and for their support, dinners and a bed whilst in Christchurch, a special thanks to Nicky and her husband Ryan.

Finally, I would like to thank my wife and best friend, Lotta, for her tireless patience, her understanding, her wisdom, her putting up with my absences and most of all, for her love.

Abbreviations used in this document

IPPS	One pulse per second
CA	Certificate authority
CAD	Computer aided design
COTS	Commercial, off-the-shelf (equipment)
CGI	Common gateway interface
CRC	Cyclic redundancy check
D.C.	Direct current
DSP	Digital signal processor
FIFO	First-in first-out
FIR	Finite impulse response
FTP	File transfer protocol
GIC	Generalised immittance converter
GPS	Global positioning system
GUI	Graphical user interface
HTML	Hypertext mark-up language
IC	Integrated circuit

I/O	Input/Output
IIR	Infinite impulse response
IP	Internet protocol
IPC	Inter-process communications
ISP	Internet service providers
ISR	Interrupt service routine
LAN	Local area network.
LED	Light emitting diode
LSB	Least significant bit
LTA	Long term average signal (energy)
LVDS	Low-voltage differential signalling
MAC	Multiply and accumulate
MEM	Micro electromechanical machine (or machining)
MODEM	Modulator/demodulator
MOQ	Minimum order quantity
MSB	Most significant bit
OEM	Original equipment manufacturer

PC	Personal computer
PCB	Printed circuit board
PPP	Point to point protocol
PSRR	Power supply rejection ratio
PSU	Power supply unit
PTC	Positive temperature coefficient
PWM	Pulse-width modulation
RT	Real-time
RTC	Real-time clock
RAM	Random access memory
RISC	Reduced instruction set computer
RLP	Radio link protocol
ROM	Read only memory
SBC	Single board computer
SFTP	Secure file transfer protocol
SLA	Sealed lead-acid
SMPS	Switch mode power supply

SMT	Surface mount technology
SMTP	Simple mail transfer protocol
SNR	Signal to noise ratio
SPI	Serial port interface
SSL	Secure sockets layer
STA	Short term average signal (energy)
TCP	Transmission control protocol
UART	Universal asynchronous receiver/transmitter
USB	Universal serial bus
UTC	Universal coordinated time
WAN	Wide area network

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1 Introduction

Because of its position on the boundary between the Pacific and the Australian tectonic plates, New Zealand experiences frequent earthquakes, at about the same rate as California. In the central and southern part of the South Island of New Zealand, the main expression of the plate boundary and the dominant geologic feature is the Alpine Fault. Recent research by Yetton [1] shows that the Alpine Fault ruptures on average about once every 260 years and that the last rupture was in 1717, nearly 290 years ago. The events are large, with rupture lengths of 400 km or more and offsets of several metres. Allowing for the variability of the interval between ruptures, Yetton estimates a probability of 65% for a M8 earthquake occurring on the fault within the next 50 years [1]. In a geological time sense, rupture is imminent, and presents an unprecedented opportunity to record shaking from a great earthquake.

Accordingly, the Geomechanics Group at Canterbury University initiated a programme to install a dense network of about 80 accelerographs in the region, supplementing the sparser National Network. This *Canterbury Strong Motion Network* would have three main objectives. The first of these is to record site effects in the highly variable and often soft sediments below the city of Christchurch. The city is built on a localised mix of fluvial and estuarine soils bounded by the sea, the volcanic Cashmere Hills and the alluvial Canterbury Plains. This mix of loose, post-glacial soils makes it difficult to predict ground response for a large seismic event. Twenty accelerographs will be deployed on a variety of formations about the city. The second objective is to study the rupture mechanism of the earthquake. To this end, a dense array of about 20 instruments will be installed near Lake Collieridge, to the east of the Alpine Fault [2]. The third aim is to observe the attenuation of strong shaking in the region, especially across the deep sediments of the Canterbury Plains. The gravel layers of the Plains, nearly one kilometre thick at Christchurch, are fairly uniform in structure and it is not clear how they would behave under very strong shaking. The off-the-shelf purchase and maintenance of the 80 or so instruments required for this Canterbury Strong Motion Network was beyond the resources of the

University. Therefore the project described in this thesis, to develop a low-cost, low-maintenance digital strong-motion accelerograph, was undertaken.

Traditionally, accelerograph instruments have relied on expensive complex mechanical/photomechanical components or expensive custom-developed electronic systems or both. The mechanical/photomechanical systems have proven to be very limited in terms of communications as well as being expensive to maintain and have consequently been largely superseded by electronic systems. The majority of common electronic systems were designed at a time when electronic components had a long availability period, and are now suffering from component sourcing issues, resulting in high service costs. As they are mostly custom designs, they are also limited in their ability to benefit from new technology, low-cost, communications systems without further expenditure.

The limited funds of the Canterbury Strong Motion Network and need for many instruments [3], means that a low-cost, long-lifetime instrument and communications system must be used. As there are no instruments fulfilling these requirements, one must be designed, produced and installed. This thesis outlines the development of a flexible, low-cost, networked acceleration datalogging (accelerograph) system. The system, known as the CUSP System, is designed to be configured for a number of possible target applications, including, but not limited to, single sensor stand-alone accelerographs, expandable multi-channel structure monitoring accelerographs and multi-sensor 'down hole' and 'free field' arrays. This research focuses only on the development of the stand-alone accelerograph, but designed with provision for the future development of the other target applications.

The network is intended to operate for at least 15-20 years. This means the instruments must be designed with an equally long life cycle. This long instrument lifetime criteria introduces the motivation for the first of two contributions to the field of scientific instrumentation design presented in this thesis – designing low-cost yet long-lifetime instrumentation at a time when component availability periods are steadily decreasing. Central to the achievement of a long life cycle is the use of a 'system of modules' approach, with all individual modules being either low-cost expendable items or standardised industrial components. This allows the system to be

rapidly reconfigured at minimal cost, to exploit new technologies and to cheaply replace failed components or those no longer available. The two main factors in achieving this are, firstly, well-specified, scalable and long-lifetime interfaces between modules, and secondly, the use of a generic operating system for the core processing platform. This replaces the usual approach of highly integrated hardware and a custom operating system with one that provides an increased level of functionality, as well as allowing the system's hardware and software to be upgraded transparently as technologies and protocols change.

A major component cost has traditionally been the acceleration transducers. The use of recently developed micromachined accelerometers, originally designed for the automotive industry, can significantly reduce this cost. Their low cost is a function of both mass production and cheap materials. Unfortunately, these sensors exhibit several undesirable characteristics that must be mitigated for seismic sensing purposes. The results of an investigation into these sensors and the resulting correction system developed presents the second contribution to the field of scientific instrumentation design that this thesis presents.

The thesis begins with a brief history of seismic monitoring, including short descriptions of some of the more important instruments of the past. A study of current instruments is presented along with their more critical specifications. A short summary of the cost and performance of current instrumentation is made and this illustrates the motivation for the CUSP Instrument. This is presented in chapter 2.

The basic requirements of a strong motion instrument are presented as a design brief in chapter 3. This is not a comprehensive specification, but rather provides a high-level framework for the development process. This design brief is the result of a review of the physical parameters to be measured and the experience of network instigators. It is verified by comparison against a design specification developed by a recognised consortium of earthquake engineers; COSMOS [4].

Chapter 4 provides a short history of the development of several prototype instruments constructed during the course of earlier work related to this research project. The main lessons learnt through this process are summarised and these

provide a basis for the decisions made in the development of the instrument presented in this thesis.

Chapter 5 presents a technical design specification derived from the high-level design brief given in chapter 3. The development of the technical specification begins by grouping the design brief's requirements into similar tasks and then discusses the consequences of implementing each requirement. The different parameters of each task are then given a minimum requirement.

Chapter 6 addresses the first of the major design issues the CUSP System must overcome; that of producing a low-cost product with a life-cycle that exceeds the availability period of its constituent components. This chapter initially defines the problems encountered when attempting to do this, then identifies a number of methods traditionally employed to mitigate them. The chapter concludes by describing a new 'system of modules' approach that presents an elegant, low-cost solution. The long life-cycle at a low cost is achieved by increasing the products tolerance to module substitution with future devices, which may have different specifications.

Chapter 7 extends the 'system of modules' approach described in chapter 6 to the CUSP System by modularising the design specification given in chapter 5. Once these modules are identified, methods to realise them are discussed and inter-module interfaces defined. The chapter concludes with a high-level map of the CUSP System.

Chapter 8 describes the characterisation and correction of the low-cost micromachined accelerometers. The chapter begins with a discussion of classic accelerometer theory and illustrates how micromachined accelerometers, with low pendulum masses and high natural frequencies, can approach the performance of 'ideal' accelerometers. Tests designed to characterise the low-cost accelerometers are then described and the results presented, indicating that, in practice, low-cost micromachined accelerometers are far from ideal. This leads to a discussion of the second major design issue that this thesis addresses; that of the correction of the poor behaviour of the low cost micromachined accelerometers.

Chapter 9 contains the work relating to the physical realisation of the CUSP System and begins by briefly outlining the implementation of the modules defined in chapter 7. The implementation phase concludes with the final product's specification. Module and overall functional testing is presented and a discussion on the success of the implementation concludes the chapter.

Chapter 10 presents the results of the research, including giving overall test results in 'real world' scenarios that highlights the strengths and weakness of the CUSP System. The final conclusions are given in chapter 11, along with an informal discussion of the research.

2 History of seismological instrumentation, review of current instrumentation and motivation for the CUSP project

The history of seismological observation instrumentation is contained in many and varied publications. The history portion of this section aims to provide a brief outline of some of the more pertinent developments in the field, thus it is not intended to be entirely comprehensive but rather to provide an overview of progress. Unless otherwise referenced, this information is drawn from two texts, Bullen and Bolt's 'An introduction to the theory of seismology' [5] and Howell's section 'Seismic Instrumentation' in 'The encyclopaedia of solid earth geophysics' [6].

2.1 *Prehistory*

The first documented device to respond to earthquake motion was a seismoscope¹, developed by Chang Heng in China in around 132AD. Heng's device is thought to have contained a pendulum, which was connected to the jaws of eight sculptured dragons heads located at the primary compass points. Each dragon's mouth contained a ball, and movement of the pendulum would release one or more of the balls that would then fall into the corresponding upturned mouth of eight sculptured toads, located below each dragon's head. Heng's belief was that the first ball released would indicate the direction of the source, indicating where damage assessment parties should best be sent.

Jean de la Haute Feuille developed the next known seismoscope in 1703. This device used mercury contained in a basin, which would slop over the edge and into surrounding cups when subjected to earthquake motion. By 1784 an Italian abbot

¹ A seismoscope is a device indicating that earth motion has occurred, some seismoscope also indicate a magnitude.

named Atanasio Cavalli improved this system and also thought to include a record of the event time by using clockwork to move a chain of collection dishes [7]; however, there is evidence that this modification was never implemented [8].

In 1751, slightly before Cavalli's timing system, Andrea Bina developed a very crude form of seismograph², which recorded a trace of the earth's motion. This instrument consisted of a pendulum suspended over a tray of fine sand. A pointer attached to the bottom of the pendulum, dipping into the sand, would trace the pendulum's motion. Forty-five years later, in 1796, Ascanio Filomarino, the Duca della Torre improved the design, including the event time by using a mechanical clock held stopped by a fine hair attached to the pendulum.

In 1855 Luigi Palmieri improved the accuracy of Feuille's and Cavalli's system, the spilled mercury now closed a stop circuit on a clock indicating event start time, while the event's duration was recorded by a trace made on a rotating drum. Palmieri was also the first to consider the vertical component of the earth's motion and in 1856 he added a mass sprung over a bowl of mercury, which upon the raising of the bowl relative to the mass, displaced the mercury and closed a circuit.

2.2 Analogue seismographs

Italian Filippo Cecchi created the first true seismograph in 1875. His instrument used two pendulums, one constrained to N-S motion and the other E-W motion. Each of these pendulums used a string and pulley system to achieve a gain of three. The vertical component was sensed by a mass suspended by a coil spring. A triggering seismoscope was used to start a timing and recording device. While his instrument was too insensitive for all but the largest events, the first known true seismograph record was produced on February 23, 1887.

² A seismograph is an instrument providing a trace of the earth's motion throughout an earthquake.

The sensitivity of the pendulums, especially to low frequency motion, was significantly increased by the application of the Zollner type suspension arrangement, developed by Hengler (1832), Gerard (1851) and Zollner (1869) for purposes of measuring tilt deflections caused by tidal changes. The Zollner suspension method involves suspending the pendulum not vertically but almost horizontally, like a gate hinged slightly off vertical so that it slowly shuts after being opened. By 1881 John Milne, Thomas Grey and James Ewing had developed a three-axis seismograph based on this pendulum arrangement, which also incorporated an accurate timing system by pressing inked clock hands onto the record. Milne continued on to create the first seismograph network based on his instrument, with roughly forty instruments spread across (largely) the British Commonwealth world.

Ernst von Rebeur-Paschwitz also developed a Zollner type instrument, based on the early work of Ewing, and added optical magnification and recording, with a consequent reduction in scribe friction. On the 17th of April 1889 a large earthquake was noted in Japan, which was recorded by von Rebeur-Paschwitz in Potsdam, Germany, thus making the first recording of a distant earthquake, albeit with only the horizontal components.

In 1898 Emil Wiechert added damping to the pendulums in order to improve the frequency response. Wiechert also developed a large mass inverted pendulum instrument, which achieved good results by virtue of the large mass's relative immunity to scribe drag. In this manner, high gain recordings could be made over a large bandwidth due to the long natural period of the large mass.

Russian Boris Galitzin (incidentally, a prince of the Russian court) developed an instrument using electromagnetics to both damp the motion of the inertial mass and to extract an electrical signal proportional to the velocity the motion [9]. A mirror attached to a galvanometer needle was used to create an optical lever to amplify this signal.

In 1922 John Anderson and Harry Wood produced a torsion seismometer³ arrangement using electromagnetic damping for recording horizontal components. The Wood-Anderson instrument used purely optical means to record the motion of the torsion mass and this instrument represented the first properly damped sensor for seismic measurements.

Hugo Benioff produced a very sensitive vertical motion variable reluctance type sensor in 1930 [10]. While the seismometer's pendulum was of traditional design, Benioff's transducer used a system similar to the telephone receivers common at that time. The transducer consisted of a permanent magnet which, when moved relative to a pair of coils attached to the pendulum, would transfer magnetic flux from one coil to the other. The output signal was, like Galitzin's sensor, proportional to the velocity of the pendulum and recorded by a galvanometer. The result was much increased gain and the sensor was capable of recording signals as low as the background seismic noise.

2.2.1 Background seismic noise

Once the sensitivity of the seismometer exceeded the background seismic noise floor, it was discovered that there is a peak to the background noise spectrum at a frequency of around 0.15-0.2Hz [11]. This is a result of various effects including the diurnal heating/cooling cycle of the earth, ocean waves and tides and cultural noise. There is up to 10000 times the difference between the peak noise amplitudes around 0.15-0.2Hz and the lowest level of the noise spectrum. This presented problems with setting the maximum gain of instruments so that the noise peak did not entirely swamp out low-level signals occurring in frequency bands above or below the peak.

Furthermore, the dynamic range of the instruments developed at this time was rather poor, the Wood-Anderson typically had a dynamic range of around 30dB and in

³ Device used to sense the motion of the earth, as opposed to a seismograph, which provides a time-history of the sensed motion.

general the best paper or film recordings had only 40dB dynamic range [12]. Later magnetic tape recorders improved this to around 60dB [13], still not enough to cover the range of expected motion amplitudes from the background seismic noise to the peak of a damaging earthquake event.

This resulted in the classification of three types of seismograph; short period, long period and strong motion, thus ensuring that all types of earth motion could be recorded adequately.

2.2.2 Long- and short-period instruments

The designs of Galitzin, Wood and Anderson and Benioff, used adjustable damping. By varying the damping factor and period of the pendulum, seismograph designers were able to shape the frequency response of the instruments. Galitzin and Benioff type instruments could also vary the period of the galvanometer. This allowed the instrument designer to create two type of instrument: long- and short-period. Long-period instruments recorded signals with frequencies below the background noise peak while short-period instrument covered the region above the peak.

The development of the World Wide Standardised Seismic Network (WWSSN) in the 1960s resulted in the large-scale deployment of such long- and short-period seismographs, principally the short-period Benioff and the long-period Sprengnether instruments. Concurrent with this, long- and short-period variants of the Wood-Anderson instrument were developed and used in many observatories.

Up until the digital revolution, increasing numbers of the electromechanical instruments used analogue tape recording mechanisms, in order to avoid the cost and complexity of photographic systems.

2.2.3 Strong motion instruments

In strong earthquakes of interest to engineers, the pendulums of sensitive instruments hit the pendulum stops and clipped the signal during strong earth motions. Thus strong motion seismographs were developed specifically for recording damaging earthquakes. This was achieved by increasing the damping and spring stiffness and consequently weak signals are lost. So while these instruments were more robust, they were also less sensitive.

Brief descriptions of several common or important instruments are given below.

2.2.3.1 USCG “Standard”, United Electro Dynamics AR-240 and Teledyne-Geotech RFT-250

The first instrument designed specifically to record strong ground motions was the United States Coast and Geographic Survey “Standard” instrument, and was principally the result of the efforts of John Ripley Freeman. Deployment started in 1932 and its first major record was from the M6.3, 1933, Long Beach, California, earthquake, where three instruments were located nearby and a peak acceleration of 0.2g was registered. By 1940 there were 52 sites equipped with “Standards” [14].

The United Electro Dynamics AR-240 followed the USCG “Standard” instrument as the backbone instrument in the U.S. This was the first commercially produced strong motion seismograph and was released in 1963 [3] and was soon joined by the RFT-250 produced by Teledyne-Geotech after their acquisition of United Electro Dynamics [14].

2.2.3.2 M.O.2 and Kinemetrics SMA-1

While both the AR-240 and the RFT-250 gave good service, they were bulky and costly instruments. When the more compact and less expensive M.O.2 and SMA-1 instruments arrived on the market in the mid to late sixties, they quickly became the dominant instruments in North America.

Dr. R Ivan Skinner developed the M.O. series of instruments in the early 1960's whilst employed in the (then) Engineering Seismology Section of the Physics and Engineering Laboratory of the Department of Scientific and Industrial Research (DSIR) in New Zealand. Seven M.O.1 instruments were developed and installed by 1966, with the M.O.2 developed to improve on this design in terms of reduced design and operational costs, as well as to provide improved performance. The first batch of 22 M.O.2 instruments was installed throughout New Zealand in 1968. In total, several hundred M.O.2 instruments were produced and were installed in diverse places including the US, Italy, Romania, Yugoslavia and Papua New Guinea.

The M.O.2 is a photomechanical strong motion seismograph, using three accelerometers with optical levers attached to their outputs. The recording system consists of 24 feet of 35mm film running at 1.5 cm per second; thus it could record up to nine 47 second records. The trigger comprised of a separate electromagnetic voltage generator operating in the vertical axis. The trigger could be adjusted and the threshold set as low as 10mg.

As usual with triggered mechanical instruments, the instrument produces no pre event information and the M.O.2 instrument takes approximately 0.1 seconds to start recording after the triggering event. The M.O.2 instrument was also capable of being connected to an external trigger allowing instruments to be coupled as an array [15]. Approximately 50 M.O.2 instruments are still in service in New Zealand in 2004, though they are being replaced with digital instrumentation as funding permits [16].

The Kinemetrics SMA-1 was released in 1970 [14]. It features photographic recording with a bandpass (1-10Hz) trigger, a full-scale range between $\pm 0.25g$ and $\pm 2g$, TCG-1 or WWVB timing and a DC to 25Hz bandwidth [17]. The records are developed and scanned into a digital file, with user assisted computerised corrections

to the record, which is generally poorly scanned due to the trace's width being inversely proportional to the acceleration (exposure is inversely proportional to the dot velocity) [18].

In addition to the difficulties with record digitisation, the SMA-1 provided no information prior to the triggering event. In fact, recording starts with a slight delay from the triggering event, thus, all information about the sensor output state before the event (tilt etc.) is lost, decreasing the accuracy of the integrated velocity and displacement records.

The SMA-1 has however proven to be a reliable instrument with many still in service today, including the small existing network of strong motion instruments operated by the University of Canterbury.

2.2.3.3 SMAC Series

A committee of researchers and engineers instigated the development of the Japanese SMAC series analogue instruments in the early to mid 1950s. Two analogue instruments were designed, after which digital instruments were produced. [19]

The SMAC-B was a mechanical analogue instrument utilising a stylus on paper recording system and was developed in 1957. It had a range of up to $\pm 1g$ and a trigger set to a level of 10mg. It had a pendulum type sensor and weighed 100kg, giving a 10Hz measurement bandwidth. It had no pre event recording capability, and a comparatively low natural frequency, with the result that erroneously low values of peak ground acceleration were recorded.

The SMAC-M was developed in 1972 to utilise force feedback sensors and electronic recording onto magnetic tape. The bandwidth was expanded to 30Hz but it lacked DC response, with a lower limit of 0.1Hz. The maximum recording level was $\pm 1g$ with an improved trigger level of 5mg. Again no pre event capability was installed.

2.3 Digital seismographs

Initially, records produced by digital instruments were preferred for computerised analysis/manipulation over analogue photographic records due to the reduction in both effort and errors introduced by the digitisation process [18]. As the digital revolution came of age, the increasing performance of analogue to digital converters and reducing storage costs increased the dynamic range and bandwidth to a point where instruments were capable of recording down to the seismic background noise floor whilst covering the entire frequency band of interest.

The development of these ‘broadband’ instruments has largely done away with the requirement for the combination of long and short period instruments. But these high performance instruments are costly, and therefore the simple strong motion recorder, focused on lower performance aimed to capture only strong shaking, still has a place.

Because this thesis is primarily concerned with the development of a strong motion instrument, the review of a selection of the most popular current instruments that completes this section focuses only on strong motion instruments.

As the strong motion instrumentation field is undergoing rapid development, one of the instruments described below (IA-1 Internet accelerograph) has been released since the inception of this research project and has been included solely for comparative interest. The specifications given are the default configuration specifications. All instruments are of the stand-alone type e.g. including internal sensors.

2.3.1 Kinematics

Kinematics [20] was originally a US company founded in 1969 and based in Pasadena, California in the U.S. but is now entirely owned by the Oyo Corporation of Japan. Kinematics has a long history developing and producing geophysical instrumentation; in 1999 they acquired Quanterra, a U.S. geophysical instrumentation company with a proven history.

Kinematics Etna

The Kinematics Etna is a typical modern digital strong motion recorder. The basic specifications of the Etna relating to the quality of the records are given in Table 1 [21].

Kinematics QDR

The Kinematics QDR is the intended low-cost replacement for the SMA-1 optomechanical strong motion recorder. The QDR offers relatively low performance compared with the other products in this comparison, especially in event detection and timing performance. The basic specifications of the QDR relating to the quality of the records are given in Table 1 [22].

2.3.2 Geotech

Geotech Instruments LLC [23] is a company based in the U.S., specialising in seismic instrumentation.

Geotech A-900A / A-900B “Strong motion recorder”

The A-900A and A-900B instruments are Geotech’s basic stand-alone strong motion seismographs. The basic specifications of the A-900A and A-900B relating to the quality of the records are given in Table 1 [24].

Geotech SMART24A “Accelerometer”

The SMART24A is a high performance strong motion accelerograph that doubles as a broadband station. The basic specifications of the SMART24A relating to the quality of the records are given in Table 1 [25].

2.3.3 Geosig

Geosig Ltd is a Swiss company specialising in geophysical instrumentation for scientific, industrial and civil engineering applications [26].

Geosig IA-1 “Internet Accelerograph”

Released July 1, 2003, the IA-1 “internet accelerograph” was developed to fulfil the requirements of the Canadian Urban Seismology Project (CUSP) proposed by the Geological Survey of Canada (G.S.C.). The IA-1 is the joint effort by Arescon, a Canadian company founded in 2000 as a “research and consultancy company specialising in environmental monitoring, instrumentation and control systems” [27], and the Geological Survey of Canada - Pacific, Sidney Subdivision [28]. Arescon were contracted to develop the data acquisition software, the communications and data serving applications while the G.S.C. developed the sensor, which uses four low-cost micromachined silicon accelerometers in parallel for each component of the three orthogonal measurement directions. The basic specifications of the IA-1 relating to the quality of the records are given in Table 1 [29].

Geosig GSR-12 and GSR-16 “Strong Motion Recorder”

The GSR12 and GSR16 represent low cost variants of Geotech’s GSR series, with low resolutions specifically targeted at the strong motion field. The basic specifications of the GSR-12 and GSR-16 relating to the quality of the records are given in Table 1 [30].

Geosig GSR-18 “Strong Motion Recorder”

The GSR-18 is a high dynamic range instrument offering improved performance over the GSR-12 and GSR-16. The basic specifications of the GSR-18 relating to the quality of the records are given in Table 1 [31].

Geosig GSR-24 “Seismic Recorder”

The GSR-24 is a dual-purpose strong motion / micro seismic recorder. The basic specifications of the GSR-25 relating to the quality of the records are given in Table 1 [32].

2.3.4 PMD/eentec

PMD/eentec [33] is a U.S. company specialising in geophysical instrumentation.

PMD/eentec SMR4000-4A “Strong Motion Accelerograph”

The SMR4000-4A is a strong motion recorder designed to achieve high performance with low power consumption. The basic specifications of the SMR400-4A relating to the quality of the records are given in Table 1 [34].

PMD/eentec SMR6102-4A “Strong Motion Accelerograph”

The SMR6102-4A is a strong motion recorder designed to achieve high performance capable of both strong and micro seismic motion recording. The basic specifications of the SMR400-4A relating to the quality of the records are given in Table 1 [35].

Table 1, Basic record specifications of a selection of current strong motion seismographs

Instrument	Maximum recorded bandwidth	RMS noise floor over bandwidth	Maximum range	Recorded dynamic range
Kinematics Etna	80Hz	15µg	±2g	18-bit
Kinematics “QDR”	25Hz	1.8mg Z 2.5mg X-Y	±1g Z ±2g X-Y	10.5-bit
Geotech A-900A	50Hz	61µg	±2g	16-bit
Geotech A-900B	50Hz	15µg	±2g	18-bit
Geotech SMART24A	50Hz	3.8µg	±2g	20-bit
Geosig IA-1	42Hz	500µg	±4g	14-bit
Geosig GSR-12	315Hz	1000µg	±2g	12-bit
Geosig GSR-16	315Hz	61µg	±2g	16-bit
Geosig GSR-18	100Hz	30µg	±4g	18-bit
Geosig GSR-24	100Hz	2µg	±2g	21-bit
PMD/eentec SMR4000-4A	50Hz	5µg	±2g	19-bit
PMD/eentec SMR6102-4A	50Hz	1µg	±2g	22bit

2.4 Motivation for the CUSP System

As discussed in the introduction, the South Island of New Zealand is overdue for a major earthquake along the Alpine Fault [1]. The introduction also describes the proposed Canterbury Strong Motion Network, that is intended to instrument the central portion of the South Island and city of Christchurch, and aims to capture three events: the rupture of the Alpine Fault, the energy transfer mechanisms of the Canterbury Plains, and the performance of the variable soils under the city of Christchurch. For this network, large numbers of low-cost instruments are required.

The requirement for a high instrument deployment density in strong motion networks [3] was highlighted by the results of the August 17, 1999 Izmit (Turkey) earthquake ($M_w=7.4$) [36] where it was clear that the deployment of a large number of basic instruments was more valuable than a smaller number of high performance instruments. Counter to this, the current trend in instrument design has been to increase the dynamic range as show in Figure 1. This has resulted in an increased cost of instrumentation, as shown in Figure 2.

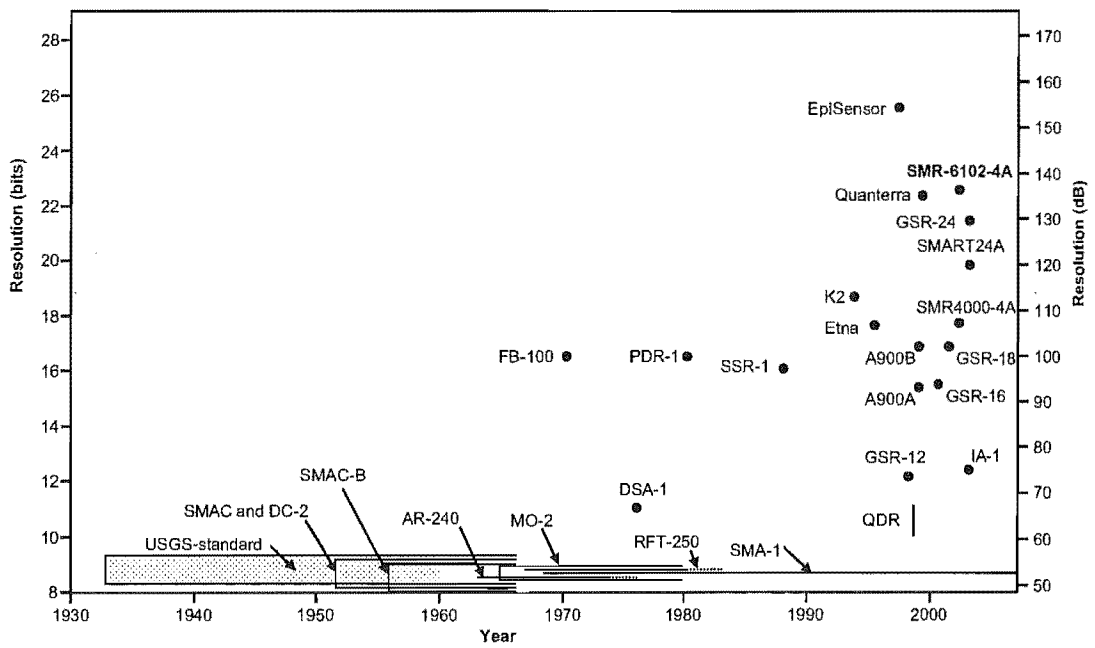


Figure 1, Comparison of dynamic ranges of selected accelerographs [updated from [3]]

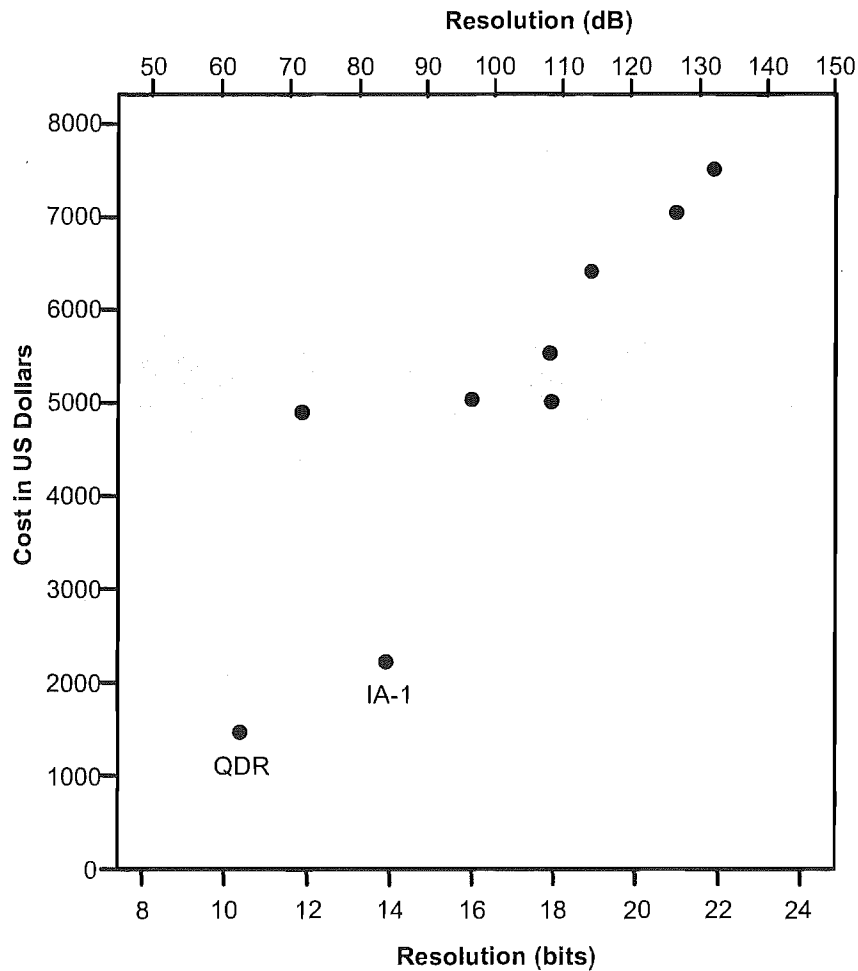


Figure 2, Correlation between purchase price of 9 instruments and recording performance

It should be noted that Figure 2 does not necessarily show the true cost of each instrument, as some of the products presented will require additional components for some intended applications. For example, some products might require additional environmental protection for some applications, thus inflating that products final cost relative to a product that already provides good protection, others may require an additional GPS receiver to meet timing requirement. These additional factors must be analysed on a case-by-case basis and is beyond the scope of this thesis.

Except for the IA-1, all the instruments presented in Figure 2 are based on proprietary circuitry and operating systems, requiring a large design effort and financial investment, which consequently needs a long product lifetime and high product costs to recoup the development costs. Unfortunately, this approach conflicts with the

current trend of decreasing component availability periods, requiring further design investment to maintain stocks of critical components in order to continue manufacture and to provide stocks for repairs. These design investments create a baseline below which the end product's performance has no effect, and is crudely interpreted as the greyed portion of Figure 2. This is the first limitation for producing a low-cost traditional seismograph instrument.

Kinometrics have attempted to break this baseline cost with the Quake Data Recorder (QDR) instrument [22]. The QDR instrument utilises low cost solid-state electronic sensors with a simple data recorder, designed for quick determination of the basic parameters of damaging events. As a result of an attempt to meet a minimum investment level, its lack of an accurate timebase (30min/year), low bandwidth (25Hz) and short event storage time (100s/event, 9 events) coupled with its marginal noise performance ($>2\text{mg}$ RMS) has resulted in it falling short of being a serious strong motion instrument.

The second limitation to producing a low-cost instrument is the cost of the motion sensors. However, the recent developments in micromachined silicon accelerometers has resulted in comparatively very low cost low-performance sensors, which, providing the baseline cost issue can be addressed, allows instrument designers to make a sensible compromise between cost and performance. The low cost has arisen from the automotive industry's demand for large numbers of low cost accelerometers for, for example, airbag deployment, active suspension, antilock braking and headlight levelling [37]. While the recent demand has dramatically reduced the price, it has equally dramatically increased the performance since their invention in 1974 [38] [39]. Unfortunately, silicon micromachined accelerometers come with penalties of both poor noise performance and poor temperature stability. For example, the Analog Devices ADXL105 accelerometer IC, typical of the low cost micromachined range, has a noise floor of 2.25mg over 100Hz bandwidth and a temperature offset drift of $\pm 100\text{mg}$ over the operating temperature range of $0\text{-}50^\circ\text{C}$ [40]. This is extremely poor compared to the Kinometrics EpiSensor ES-T which has a noise level of $0.07\mu\text{g}$ RMS over a 100Hz bandwidth and a temperature drift of $\pm 12.5\text{mg}$ over $0\text{-}50^\circ\text{C}$ [41].

At the time of the CUSP project's inception in 1998 the IA-1 instrument featured in this chapter was not available, and the gap in the range of low cost instruments with about 12-14 bits of resolution lead to the decision to pursue the development of an in-house instrument. The motivation for the CUSP System is to produce an instrument with recording, communication and operating performance comparable to the high-end instruments but, by careful design to avoid the baseline cost issues and by capitalising on the low-cost MEMS accelerometers, to trade off sensor resolution for cost. This allows the Canterbury Strong Motion Network to realise its goal of instrument deployment density within its constrained budget. The incorporation of modular sensors provides scope for future performance enhancements as budgeting or sensor improvement allows. The design also seeks to reduce maintenance costs by incorporating Internet communications for monitoring instrument health and for transferring records.

3 Development of the design brief

3.1 Introduction

The design brief is the first document produced when designing an instrumentation system. It records the practicable design parameters that represent the best compromise between the typically conflicting features desired by the project instigators⁴. Usually, several interview, research and review iterations are required to resolve the optimal design parameters. The design brief is not a concrete document, and may be adjusted later in the design cycle as unexpected improvements and limitations arise in the course of the development process. However, changes to the design brief must be exercised with caution, as, while it is important to ensure an efficient and economic final product, constant re-specification may expand the development period until development costs dominate the budget.

Since the CUSP System is specifically targeted for the proposed Canterbury Strong Motion Network, the project instigators are the members of the Geomechanics Group at the University of Canterbury, which is the driving force behind the network. Additional consultation was sought from the staff of Geonet, along with input from Dr. Jarg Pettinga.

This chapter does not show the iterative development process, but attempts to present the end result, with some indication of the compromises made. The chapter starts with a brief description of the desired features, followed with a review of the parameters of the earth motions that the instrument must record, which leads to the data acquisition parameters. This is followed by the practicable means of operation, with the storage, interrogation and physical parameters being discussed. The design brief development concludes with a review and comparison with an industrial instrumentation design specification, providing an independent 'reality check'.

⁴ i.e. infinite performance at zero cost

3.2 Design brief development

In broad terms, the instrument must gather useful information on the motion of the earth in order to increase the knowledge of the energy release mechanisms of the Alpine Fault as well as the seismic energy transfer mechanisms of the Canterbury Plains and the soils beneath the city of Christchurch. To faithfully record the earth's motion, the properties of the motion and methods of measuring and recording it need to be understood. The properties of the motion are defined as the earth's motion parameters, the measurement process as signal (or data) acquisition and the type and methods of the recording process as recording parameters. More mundane parameters that also need definition are the user interface and the physical operating parameters.

3.2.1 The project instigators desired features

The list of desired features ensuing from the iterative interview, research and review process are recorded as:

- Measure earth motions to as good a resolution as possible given the financial constraint to match or better the equivalent price of the Kinemetrics SMA-1 released in the 1970s.
- Store all events of significance in non-volatile media, for at least 2000 seconds. This is based on an anticipated single 200-second main event and thirty 60-second preshocks or aftershocks. The records must contain a short period of pre-event and post- event data.
- Provide accurate event timing, at least to 10ms absolute error from universal coordinated time (UTC).
- Provide a means of remote data access, along with remote configuration and diagnostics, over telephone, radio networks or cellular data links.
- Operate for at least three days without primary power.
- Operate in harsh environments, for example in remote outdoor locations.
- The instrument should be designed for a 15-20 year service lifetime.

3.2.2 Review of earth motion parameters and consequence signal acquisition requirements

The general characteristics of earthquake motion during a seismic event are well known. The central parameters affecting the design of the signal acquisition system are the range of seismic waves frequencies (bandwidth), the seismic waves amplitude range (dynamic range), and the nature of the recorded property (displacement, acceleration etc.).

Mathematical manipulation via integration or differentiation allows recordings made in displacement, velocity or acceleration to be transformed to any of the other properties (i.e. the integral of acceleration is velocity). Thus, subject to conditions of quality of recording, the property recorded can be any of the three linear motion measurements. Typically acceleration is measured, as this is the easiest property to acquire a high accuracy electrical signal of [42], furthermore, accelerometers are typically cheaper and more robust than velocity or displacement sensors. Three orthogonal axes are required to uniquely define a three-dimensional motion.

The expected peak acceleration is somewhat harder to define, as the underlying geological structures affect the transmission of seismic energy to the surface [42], typically strong motion instruments have up to $\pm 2g$ range [43]. The largest US earthquake accurately recorded was the 1994 Northridge event in California, with a peak acceleration around $1.8g$ [44]. This was later determined to be unusual and a result of localised ground effects [45], but the maximum recorded peak acceleration appears to have increased as the number of deployed instruments has increased [36]. A more conservative maximum range limit might be more appropriately set at $\pm 3g$ to ensure that all motion at all sites is recorded without clipping, and that the magnified responses of structures can be fully recorded.

The minimum resolution for 'strong motion' seismogram is typically defined as $5mg$ [42] [46] thus defining the required resolution. However, it is desirable to improve upon this as much as possible, especially in regions of lower seismicity and where it is wished to study site effects using the Nakamura method.

The frequency range of seismic waves has a typical upper limit of between 10 and 50Hz. [47] [46]. Since one of the intended applications the CUSP System is use on bedrock and within the earthquakes near-field where high frequency components may be present, this frequency is increased to 80Hz. The lower limit is defined as 0Hz in order to record permanent displacements.

While it is impossible to achieve a perfectly linear phase and signal response, little information is available to define the maximum acceptable errors. A consensus appears that up to $\pm 4^\circ$ phase linearity and $\pm 4\%$ signal linearity can be tolerated for seismic analysis over the instrument's measurement band [43]. This is a rather outdated source and significantly better performance can be realised with modern technology.

Traditionally, sensors represent a significant portion of the budget in accelerograph construction. As discussed in section 2.4, the use of low cost micromachined accelerometers allows the CUSP System to significantly reduce the overall system cost. Due to the relative immaturity of the MEMS technology, it would be prudent to physically isolate the sensor system to allow for upgrades as the technology matures and improved devices become available.

The analyses of minimum signal measurement parameters can be summarised as,

- Three-axis orthogonal linear acceleration measurement
- 0-80Hz measurement bandwidth
- $\geq \pm 3g$ peak acceleration before clipping
- $\leq \pm 0.005g$ minimum resolution
- $\pm 4^\circ$ phase linearity and $\pm 4\%$ signal linearity over the instruments measurement bandwidth.
- The sensor should be physically separated from the data possessing system to enable higher performance sensors to be easily integrated in later generations of instrument.
- The interface between the data acquisition system and the data processor system should be scalable to accommodate improved resolution sensors.

3.2.3 Recording parameters

In order to minimise the quantity of data gathered, the instrument should operate on a triggered basis and therefore only record data during a significant event i.e. motion above some predefined threshold [47].

Subsequent analysis of the recorded data will involve integration to provide velocity and displacement signals. It is therefore crucial that information prior to the triggering event is gathered to provide the initial conditions for the integration. The pre-event recording length is given as a minimum of 2.5 seconds [46]. This rather short pre-event period is the minimum and an adjustable pre-event length up to an upper limit of 60s is desirable. The length of data recorded after a significant event is set by the storage capacity of the instrument, and hence is not defined. The instrument should, however, record post-event data for a minimum of 10s after any event.

The sample rate must be high enough to record the entire measurement bandwidth; therefore due to the Nyquist limit, the minimum sample rate should be over twice the measurement bandwidth of 80Hz. Allowing for a 20Hz anti-alias filter transition bandwidth, the recorded sample rate should then be 200Hz, which represents a compromise between ease of the realisation of the filter and data storage/transmission efficiency.

Historically, the triggering of the recording process usually occurs when an absolute threshold is exceeded, typically 10mg [43]. More advanced forms of triggers are often provided on more recent instruments. These are of filtered absolute-level type where the measured signal is lowpass, highpass or bandpass filtered prior to level detection. The 'short-term to long-term average power ratio' (STA/LTA) type adaptive trigger is not considered useful in this design due to the high sensor noise floor; the changes to the background noise floor are swamped by the sensor noise. However, consideration should be made for the future inclusion of an STA/LTA triggering scheme.

The storage of earthquake records requires some form of non-volatile memory. The minimum quantity of data that can be stored should exceed 2000 seconds. This consists of an estimate of one large-magnitude event lasting for 200s, and thirty 60s preshocks or aftershocks. In practice, the availability of cheap memory should allow this minimum value to be far exceeded.

As the sensors may be replaced with higher resolution units in the future, the resolution of the recorder system must cater for this. Therefore, the minimum dynamic range of the recorder should be in excess of 16 bits, and preferably 18 bits.

To allow for record identification, as well as for many of the tasks of classical seismology, i.e. epicentral location, the timing of records is critical and must be linked to universal time (UTC). The maximum deviation from UTC is set to ± 10 ms in the desired features list presenting in section 3.2.1.

The requirements of the recording system are summarised as:

- Record only during significant ground motion.
- 200Hz sample rate
- Recording triggered by absolute measured acceleration (allpass, highpass, lowpass or bandpass filtered).
- 10mg trigger sensitivity, upwards adjustable.
- Provision for future implementation of STA/LTA triggering.
- Record between 2.5 and 60 seconds of pre-event data preceding triggering.
- Continue recording for at least 10s after the motion falls below the triggering threshold.
- 2000s of non-volatile data storage.
- 16 to 18-bit resolution capability from interface through to storage.
- ± 10 ms timing error from UTC

3.2.4 User interface and communications parameters

A communication system is needed to fulfil the desire to retrieve data and adjust operating settings on a remote instrument. Being able to interrogate the instrument remotely via telephony or wireless networks results in a significant reduction in the costs associated with periodic physical visits. If frequent visits are to be eliminated, functionality is required to perform remote diagnostics, such as battery condition monitoring.

The user interface must be simple and intuitive to use, helping to prevent errors due to operator confusion. In order to minimise the costs associated with custom interface development and to maximise deployment flexibility, the interface should not require any proprietary client-side software or communications protocols.

The basic user interface and communications specifications are given as

- Secure remote interface access (wireless or telephone, encryption)
- Simple, intuitive interface structure
- Access to stored data
- Access to diagnostics information
- Access to configuration parameters
- Preferable to utilise existing standard protocols/interfaces
- Optional automatic transfer of health report or new data records

3.2.5 Physical parameters

The physical requirements for the instrument are best defined by considering the intended deployment sites. Typically the instruments:

- Will be placed in a covered situation, but may be exposed to some water from leaks or flooding etc.
- Will have a primary power supply that may fail during a severe event
- May be subjected to falling debris
- Will be protected from vandalism but may be tampered with by curious site owners
- Will not be subjected to abnormal temperatures, but must withstand normal ambient temperature range of -10 to $+45$ degrees
- Will not be subjected to abnormal (i.e. condensing) humidity, but must withstand normal range of 5 to 95% relative humidity.

These parameters result in the need for a splash proof enclosure capable of being locked and strong enough to survive moderate debris cover. The need for a back up power supply is indicated; this should last for a minimum of three days to allow time for recording aftershocks and the site operator to change batteries or for the restoration of primary power.

The resultant requirements are thus

- Splash proof enclosure
- Lockable
- Moderately strong
- Have backup power supply capability
- Operate over -10 to $+45$ degrees ambient temperatures
- Operate over 5 to 95% relative humidity.
- 15-20 year service lifetime

3.3 *Verification of the design brief*

3.3.1 Review against industry requirements

As the CUSP system is a low cost instrument capitalising on budget sensors, a direct comparison of competing units is not possible. However, comparisons on the communications, storage and processing parameters can be made. Further, since scope is provided for improved resolution sensors (section 3.2.2), some form of sensor comparison can be made on the grounds of anticipated future enhancements.

The Consortium of Organizations for Strong-Motion Observations Systems (COSMOS) is an organization whose mission is to “To expand and modernize significantly the acquisition and application of strong-motion data in order to increase public safety from earthquakes” [4]. COSMOS has developed a basic specification for strong motion instrumentation that is generally followed by academia and the industry. The basic COSMOS specifications at the level of the design brief along with the comparable CUSP System design goals are given in Table 2 [48].

Table 2, Specifications of the COSMOS recommended instrumentation and the CUSP System

Parameter	COSMOS	CUSP
Peak acceleration	±2g	±3g
Dynamic range	18bit	18bit recording capable
Noise floor	0.02mg RMS (0-40Hz)	5mg RMS (0-80Hz)
Sample rate	200Hz	200Hz
Communications	Continuous or dial-out remote	Dial-out remote
Timing error	±0.5ms UTC	±10ms UTC
Record storage	2 hours	2000s (33m)
Trigger	1-5mg 0.1-12Hz	10+mg, high-, low-, all- and band-pass filtered
Post event recording	>60s	>10s
Pre-event recording	>30s	2.5-60s
Power supply	>4 days	External battery of non-limited capacity

Table 2 shows a good comparison to the COSMOS specified strong motion instrument, except for the sensor resolution. As the CUSP System incorporates scope for sensors upgrades, the modification of the timing and record storage size/buffer formats will bring it up to the COSMOS specification.

3.3.2 Interviews

The final design brief was presented for review by the people listed in section 3.1 and subsequent interviews were made. The design brief was then accepted as a reasonable basis for initiating further work.

4 Instrument design history and lessons learnt along the way

4.1 Initial sensor proving

During the summer lecture break of 1996, the author developed a prototype instrument to test the suitability of the low-cost ‘airbag’ MEMS accelerometers for seismic monitoring purposes. This prototype instrument utilised a personal computer based data acquisition system and minimal signal processing. Triggering was performed by sensing the raw acceleration and data was stored in a text file. The result of this work proved the sensors provided an acceptable performance level (5mg RMS noise floor) at a very low price – at the time around USD20 per accelerometer. The design was abandoned due to the heavy reliance on full sized computer components, with their inherent bulk and need for a continuous and high capacity power source.

4.2 First stand-alone instrument

Encouraged by the initial work, a final year electronic engineering project was undertaken by the author to produce a standalone instrument using the low-cost sensors.

Temperature drift issues were addressed by the adoption of a long-term-average subtraction method, which provided the sensors with a stable baseline. This functioned by mounting the sensors on a large aluminium block with a high thermal inertia. The high thermal inertia slowed any temperature changes such that the temperature error over the period of the long-term-average was negligible. While effective, this approach required a rather expensive thermal block, both in materials and machining costs, and did not offer true DC monitoring.

As the project neared completion, several other issues arose that ultimately proved the design unsuitable. The triggering system was too crude, as it lacked any filtering, and as the microprocessor was at the limits of its performance, no additional capacity was available for improvement. Furthermore, the timing system relied on a simple crystal-based clock and was therefore inaccurate over the operational temperature range that was expected. Another major design failing was the limited communication interface, being a direct connection to a PC via the serial communications port.

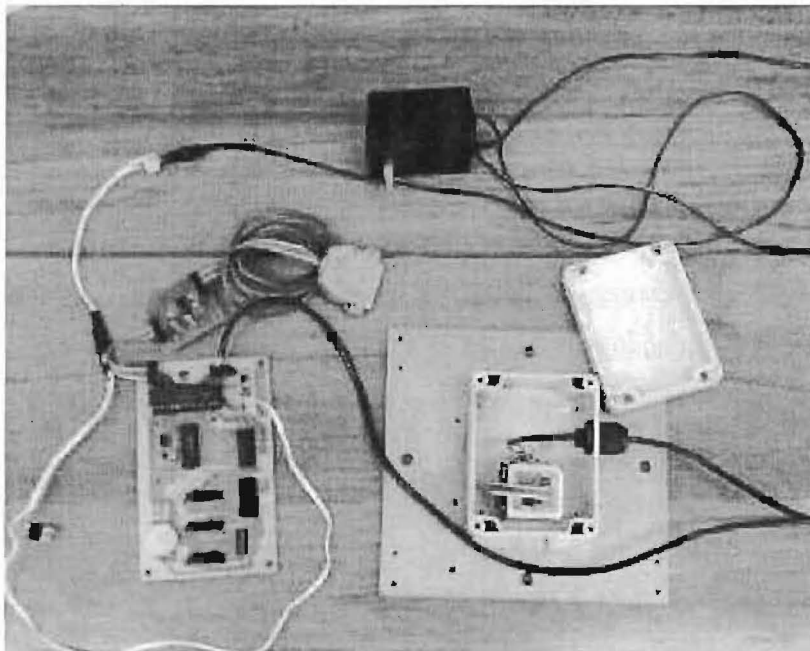


Figure 3, The 1997 instrument, produced as part of authors final year undergraduate project showing communications interface, sample block (in plastic box) and microprocessor circuit.

4.3 High performance stand-alone instrument

The project was extended to a Masters of Engineering research topic, undertaken again by the author⁵. It was determined that two things were required; more signal processing power for the instrument and additional funding and support for the development. A commercial partner was approached to provide electronic design expertise, advice on professional engineering techniques and also to qualify the project for funding through the New Zealand Government's Graduate Research in Industry Fellowship (GRIF) scheme.

To increase the processing power, various options were examined from single board industrial computers (SBCs) to embedded multiprocessor units. Eventually, for reasons of cost, performance and availability, a Texas Instruments TMS320C32 32-bit floating point Digital Signal Processor (DSP) was chosen as the core of the instrument. Also, a global positioning system (GPS) receiver was included to improve the timing accuracy.

Design improvements were made to ensure the system could be maintained or upgraded over time; for example, the sensor system was separated from the processing system, permitting sensors upgrades as new versions became available. Processor-independent control of the sampling process was implemented to ensure accurate sample timing and reduced sample jitter. Dual communications ports were added to allow concurrent local and remote communications, while the communications was improved to provide telephone modem dial-in and dial-out support, with a dial-on-event scheme. A power management strategy was added to allow battery status monitoring and controlled system shutdown. Expansion ports were supplied to permit many instruments to be chained together for use in arrays of for structure monitoring.

⁵ This research project was later extended from a masters programme to a doctoral study programme. Therefore, while the masters research results were compiled into a thesis, this was not submitted.

A prototype was assembled using a commercial processor evaluation board. When correct operation was verified, a single board version was designed using a state-of-the-art 6-layer printed circuit board (PCB) and surface mount technology (SMT). Figure 4 and Figure 5 show the prototype and final versions of the circuit board; Figure 6 shows the completed unit in a display case, with watertight connectors for external interfaces.

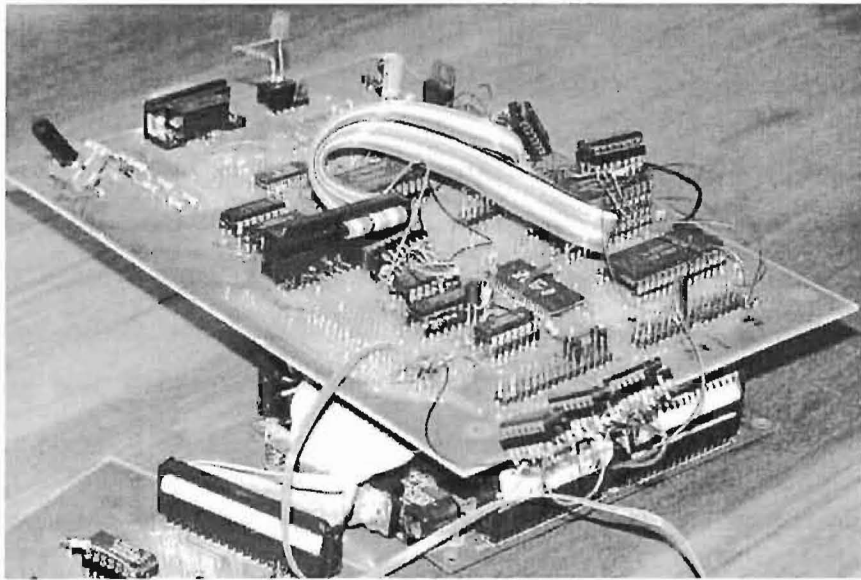


Figure 4, Hardware prototype of the DSP version

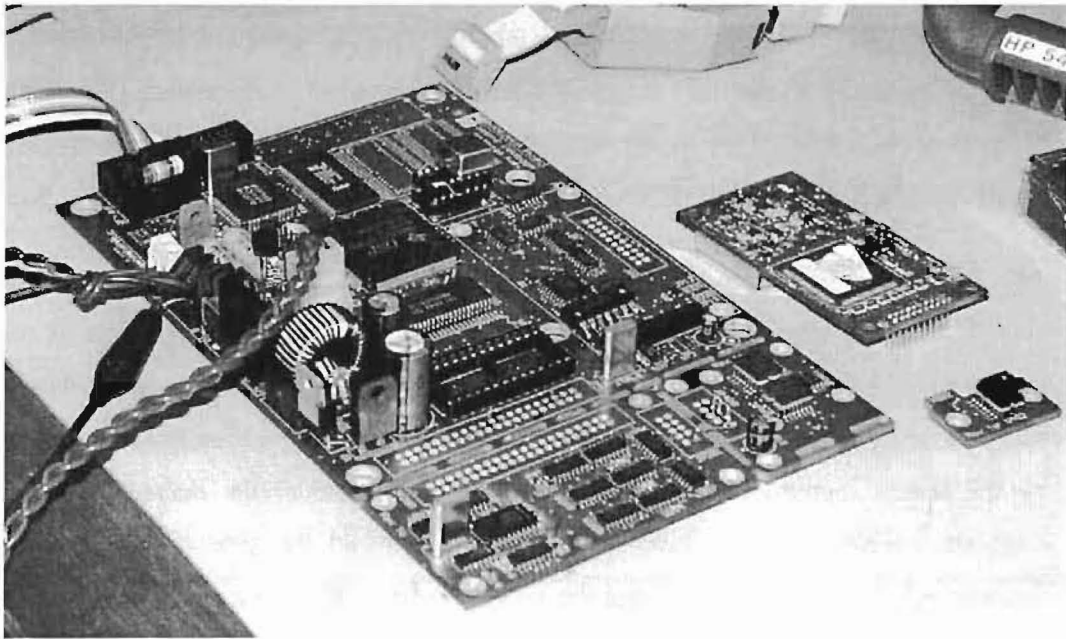


Figure 5, Completed DSP based instrument with GPS alongside.



Figure 6, Completed DSP based instrument in case with display window on top.

Between the construction of the prototype and the layout of the single board version, a new generation of sensor was released offering double the performance (2mg RMS noise floor) at a fifth of the power consumption (2mA vs. 10mA). This sensor was incorporated into the final version.

This instrument had a considerable processing power advantage over the previous version and the triggering was upgraded to employ absolute level (filtered and unfiltered) and also STA/LTA triggering. Temperature-dependant drift in the sensors was slowed by a smaller thermal mass and corrected by using a lookup table indexed by the sensor temperature, measured by a digital thermometer embedded in the sampling circuit's thermal mass. This method reduced the size required for the thermal sink, as it only had to hold the three sensors at the same temperature as the thermometer.

While this instrument offered much of the performance that was required, it suffered from the problems of component availability and obsolescence. During the period between development and the intended construction time several components became unavailable and others were listed as 'life time buys'⁶. Furthermore, the manufacturing price was significantly higher than anticipated. These problems were considered serious enough to abandon the project.

The complete development of this instrument is provided in the authors attached, but not submitted (see footnote 5), masters thesis, "The Development of a Low-Cost Strong Motion Seismic Datalogger Instrument and a Central Monitoring Application" [49].

⁶ The manufacturer is in the discontinuation process and will not be replacing current stocks.

4.4 First single board computer based instrument

With the abandonment of the DSP based instrument, a decision was made to put the research on hold and look at possible alternative approaches that would avoid the issues of component obsolescence in complex designs, and the high manufacturing costs associated with low volume production runs.

Whilst initially rejected, it was noted that during the DSP based design's two year development period, single board computers (SBC) had both significantly dropped in price and improved in performance. The use of a SBC neatly sidesteps the problems of component obsolescence and manufacturing expenses while improving long-term reliability. The cost and reliability advantages arise from the use of finely tuned mass production methods, while component obsolescence is mitigated by the heavy industry commitment and investment in proven architectures, providing the same functionality between manufacturers and technologies and confidence in an ongoing supply.

A test platform was constructed from a desktop PC, which formed an ideal development base, being compatible with the x86 SBCs. In order to ease development work, MS-DOS was utilised for file handling tasks. MS-DOS is a single-tasking operating system, which was required to ensure that the instruments software had control over the timing of the sampling process.

New sensor circuits were developed which were based on the circuits used in the DSP design. The new circuits included some analogue signal processing components and a microprocessor for sampling control that also contained a lookup table for temperature correction. This resulted in a standalone sensor, producing formatted and corrected data. An ISA-bus interface card was also developed to allow the SBC to interface to multiple sensor circuits and also included a GPS timing interface decoder and controller. These circuits are shown in Figure 7 and Figure 8. Figure 7 shows the data acquisition and transducer circuit that connects to the ISA bus board (unfortunately none of these circuits exist in their entirety now, so an image of a partially disassembled circuit will have to suffice) while Figure 8 shows the multiple-

input ISA bus board. Note the use of RJ45 connectors, allowing the use of low cost Ethernet cable and connectors.

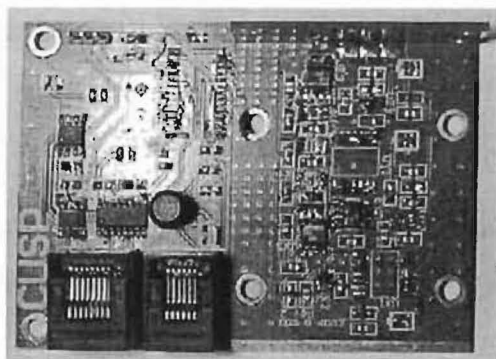


Figure 7, Partially disassembled transducer and data acquisition circuit for connection to the ISA bus interface card

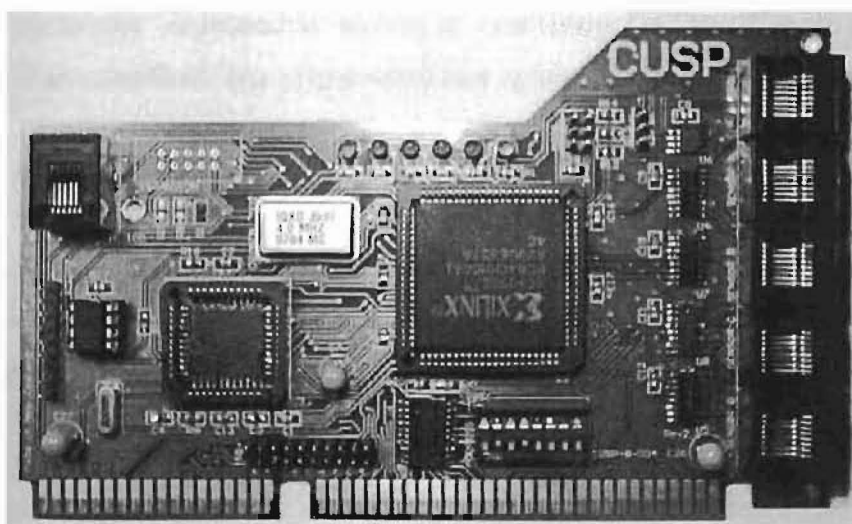


Figure 8, ISA bus interface card to transducer and data acquisition circuits

The bulk of the software code was imported from the DSP version, as most programming had been done in the ANSI C language. Several advances were made, principally the addition of Ethernet communications using a custom-coded HTTP web server for data transfer, and SMTP email delivery for event notification. PPP telephone dialup support was also coded for standardised remote data gathering.

Achieving real-time performance to sample data without loss was a major difficulty. No manufacturer-supplied driver routines for MS-DOS could be used due to their

unpredictable handling of interrupts. This resulted in the need to develop all of the drivers required by the system, including network card drivers. This had two adverse effects:

- As the quantity of the code required to perform the growing number of tasks grew, it was becoming unwieldy to debug, resulting in errors.
- The system was becoming locked to the hardware for which the drivers had been specifically programmed.

An industrial x86 based SBC was successfully evaluated to transfer the system from the full-sized desktop PC to something suitable for a field instrument. Also, the dedicated multi-channel ISA bus circuit board was eliminated by limiting the number of channels to just one and by modifying the sensor circuits to utilise the standard PC RS232 serial port interface.

The final cased unit, which included a small backup battery and power supply, is shown in Figure 9.



Figure 9, Test platform for a SBC based instrument

4.5 Lessons learnt for future work

The development of the four previous instruments provided valuable experience in the design of seismic datalogging instrumentation. The most important points being:

- Due to the relatively high performance required by seismic recording (e.g. c.f. once-daily river level monitoring), complex and high performance hardware platforms are required to provide the necessary processing power.
- While the seismograph specific software routines were transferable to different hardware platforms, hardware specific functions were not, resulting in high maintenance overheads when any modifications were required.
- The effects of the low-cost MEMS accelerometer are correctable, but with considerable effort both in the correction process as well as characterisation.
- Accurate timing with free-running clocks is difficult to achieve without frequent synchronisation, and the use of remote clock resetting can be more expensive overall than a GPS clock, if the communications are not free of cost.

The first of these points presents the most serious design issue. It was clear that customised circuitry was both time-consuming and expensive to develop and risky to use, since there is no guarantee that components will remain available for any length of time. This enforces future redesign work and/or the pre-purchase of anticipated future quantities. Furthermore, the relatively small production runs anticipated makes manufacturing expensive since the set-up costs for circuit board manufacturing and assembly are fixed and the costs of components in small quantities is significantly higher than for bulk quantities. The development and debug time and revision numbers required to design a bug-free processor system are also serious considerations.

The adoption of a standard industrial SBC nicely sidestepped these issues. Thier mass production and widespread availability results in a low-cost standardised product. The diversity of manufacturers and commitment by industry will result in long-term availability, even if the x86 platform is being ‘emulated’ in a code-compatible shell.

However, unless the drivers supplied by the manufacturers can be used, the benefits of the x86 SBC's ability to adapt to new hardware implementations and technologies are lost.

The use of MEMS accelerometers results in a low cost transducer. The effects of temperature can be reduced, but this requires careful and time-consuming calibration and a not inconsiderable quantity of processing power (for an integer microcontroller). The use of GPS based timing is not an expensive option given the continuing reduction in the cost of GPS receivers, but it does require an additional high performance interface to be incorporated into the design.

5 Development of a design specification

5.1 Introduction

The high-level outline of the requirements for the CUSP System presented in chapter 3 treats the instrument as a ‘black-box’, specifying what it should do at an end-user level. To realise the design brief, the high-level requirements must be reviewed with consideration not only to what the instrument should do, but also how it should do it. The consequences of any differing approaches must be discussed and a design-oriented specification written that provides the design process with clear guidelines as to the approaches that should be taken and the minimum specifications the various parameters of the instrument must meet. This chapter divides the design brief into related tasks and discusses them in the following major sections

- Data acquisition
- Recording parameters
- User interface parameters
- Physical parameters

The sections conclude with a summary of the discussion and list the parameters of the design specification.

5.2 Data acquisition

A summary of the signal parameters of the system-requirements brief is shown in Table 3. In addition to these numerical parameters, the data acquisition system must accommodate future improvements to data resolution with minimal cost and changes to the remainder of the CUSP System.

Table 3, Data acquisition system signal parameters

Sensor	Triaxial acceleration
Recording bandwidth	0-80Hz
Peak range	$\geq \pm 3g$
Resolution	$\leq \pm 0.005g$
Phase linearity	$\pm 4^\circ$
Signal linearity	$\pm 4\%$

In order to record acceleration with a digital system, the analogue signal must be converted to a digital representation. This process is called ‘analogue to digital conversion’ or simply ‘A/D conversion’. A/D conversion of dynamic signals involves acquiring a digital representation of the signal at a fixed rate called the sample rate. The sample rate determines the maximum bandwidth of the signal that can be converted, due to the Nyquist criterion:

Any signal components present before sampling that have a frequency greater than one half of the sampling frequency will be aliased back into the sampled signal at a lower frequency causing distortion. The limit of one half the sampling frequency is known as the Nyquist frequency (after [50]).

This condition requires that all components of the motion signal with a frequency above the Nyquist frequency must be filtered out. Filtering according to the signal parameters given in Table 3 does not present significant difficulty except for the very tight requirement for both amplitude and phase linearity. To minimise the quantity of stored data, the signal must be sampled at a rate close to the Nyquist limit, necessitating a high roll-off analogue antialias filter. The work performed on the DSP based design described in chapter 4 [49] demonstrated the difficulty in achieving a minimal sample rate whilst maintaining both amplitude and phase linearity. The conclusions show that filter linearity is highly dependant on the filter design and generally behaves poorly nearing the filters cut-off point. Furthermore, high performance filters are sensitive to component tolerances and temperature changes, causing deviations from a repeatable response.

Considering that a digital filter can be designed with both a perfectly linear phase response (i.e. a fixed time delay) and a very narrow transition band, a solution to this problem is to:

1. Use a slow roll-off analogue filter with high linearity and stability,
2. Sample the data at a higher rate to meet the new Nyquist frequency,
3. Apply a digital filter to the oversampled data, reducing the bandwidth of the signal to an optimal value,
4. Decimate the filtered digital data stream to maximise the efficiency of data processing and storage.

This shifts the filters region of poor response upwards and out of the final recorded frequency range but enforces oversampling of the signal to meet the higher Nyquist limit. The cost of this approach is the need for more digital signal processing performance, but provided the processing power is available, the simplification of the analogue filter, the increased stability and the performance improvements are justification.

The results of the investigation into analogue filters for the DSP based design show that the phase response of both Butterworth and Chebyshev filters is approximately

linear for only the first 5% of the passband [49]. Delay equalisation circuits can extend the linear phase region to almost half the passband [51], but do not address the issues of sensitivity to component tolerances and changes over temperature. Conversely, linear-phase filters such as the Bessel filter suffer from the same effects but applied to the amplitude rather than the phase response. Compromise type filters offer something in between, but even a well-designed filter such as optimally configured generalised immittance converter (GIC) filter cannot offer both linear amplitude and phase responses for more than first half of its passband [52]. Given that a practicable analogue filter will have, at best, an acceptable passband response limited to the first half of the designed passband, and a transition band equal to the passband width, the minimum sample rate must be four times that required for an ideal filter. For the recording bandwidth of 80Hz given in Table 3, and allowing a 20Hz digital filter transition band, the minimum sample rate must be 200Hz. With an oversampling ratio of four, the sample rate becomes 800Hz.

From the definition of the decibel unit, resolution in decibels (dB) is given by the expression

$$resolution = 20 \cdot \log \frac{signal_{max}}{signal_{min}}$$

With a resolution of 5mg and a range of $\pm 3g$, the signal conversion resolution must be just over 61dB, which is equivalent to just over 10 bits of digital data. However, because the system requirement brief (chapter 3) states that the recording system should be capable of recording 16-18 bits of data resolution, it would be prudent to ensure that the interface between the data acquisition and the recording circuitry can handle 18 bit data transfers.

As chapter 4 shows, the low-cost MEMS accelerometers exhibit deviations from ideal performance, especially in terms of temperature stability, and consequently require some form of correction process. In addition, the CUSP System must provide scope for changing the sensors to better versions at a later date with minimal changes and costs; this makes it logical to perform (or to include all the parameters for) the correction process within the replaceable portion of the data acquisition circuitry.

As a result of requiring a digital filter in the sampling process, 16-18 bits of data resolution and the correction of the MEMS sensor errors, the signal path between the output of the accelerometer and the storage in non-volatile media presents heavy data processing requirements.

For the digital filter, the combination of the linear phase requirement and the small transition band forces the use of a linear phase filter with a steep roll-off response. Thus, a finite impulse response (FIR) filter is required, resulting in a large number of filter taps. Matlab modelling of a filter that meets the sample rate, passband, stopband and attenuation requirements yields a filter with over 180 taps. Implementing this filter requires the summation of 180 multiplications at the data storage rate of 200Hz for each of the three channels. Therefore, nearly 110000 multiply-accumulate (MAC) operations must occur each second with at least 16-bit data and multiplicands. This results in a processor loading greater than that of typical microcontroller. For example, a Microchip PIC16F876 processor clocked at 20MHz can perform some 5 million instructions per second (MIPS); however, experimentation with coding for a single 16-bit MAC cycle takes around 300 instructions cycles to achieve, thus reducing the throughput to less than 15000 MACs per second (appendix A).

It is clear then that greater processing power than provided by a simple microprocessor is required for the digital filter alone. Options to provide the required processing power include multiple processors, digital signal processors with dedicated MAC units, or simply a more powerful processor. A better solution, however, is to share the processing tasks, allowing a cheap microprocessor to be used for controlling the data acquisition and MEMS sensor error-correction process, and then performing the heavy filtering work in another processor, that can also perform the overall control and coordination of the CUSP System, as well as other tasks such as the communications and record detection. This approach meets the requirement for a replaceable data acquisition system (i.e. low-cost) while still providing the necessary processing facilities.

The minimum design specifications for the data acquisition process are summarised as:

- 3 channels of acceleration data.
- $\pm 3g$ signal magnitude response.
- $\pm 0.005g$ resolution.
- $< \pm 4^\circ$ phase linearity over signals recorded bandwidth.
- $< \pm 4\%$ signal linearity over signals recorded bandwidth.
- High magnitude and phase linearity antialias filters.
- 80Hz signal recording bandwidth.
- 10 bits of sensor resolution (A/D conversion).
- 800Hz sample rate (A/D conversion).
- Linear phase digital filter to 80Hz bandwidth.
- 4X decimation for signal storage.
- 18 bit digital data transfer interface.
- Replaceable sensor module to allow for sensor upgrades.
- Correction of any accelerometer output errors within the replaceable module.
- Use of an external, high-performance processor for heavy signal processing.

5.3 Recording parameters

Table 4 shows the desired recording parameters defined in the system requirements brief.

Table 4, Recording parameters defined in system requirements brief

Data storage rate	200 samples per second
Recording	Triggered (only during significant ground motion)
Trigger	Absolute measured acceleration (allpass, highpass, lowpass or bandpass filtered).

Pre event memory	Between 2.5 and 60 seconds of data
Post event memory	At least 10s of data after the triggering event
Storage quantity	2000s, non-volatile
Data format	16-18-bit resolution from interface through to storage
Event timing	± 10 ms timing error from UTC

Because a hardware implementation of the recording triggers, with filters, would be complex, expensive and impossible to remotely adjust, this task is better performed in a software routine with digital filters. Since the necessary processing facilities exist as part of the data acquisition process, adopting this approach results in an adjustable, flexible and low-cost solution.

The minimum quantity of buffer memory needed for storing pre-event data is determined from the maximum length of pre-event data required and the data storage sample rate. 60 seconds of data at 200 samples per second over three channels of 18 bit data represents some 108 kilobytes of 8-bit memory.

The quantity of non-volatile storage is determined again from the data storage sample rate and the length of storage required. 2000 seconds of non-volatile storage for three channels of 18 bit data at 200 samples per second equates to some 3.6 megabytes of data. To this, file headers and footers must be added to each record, which should contain the recording parameters, instrument configuration data and timing information so that records can be uniquely identified and the operating parameters at the time of the recording determined. This would then extend the 3.6 megabytes to an estimated 4 megabytes. This defines the minimum quantity of non-volatile data storage space to be provided.

Accurate record timing presents a design issue requiring special consideration. It is difficult to provide accurate time information from a free running clock over a significant time interval. Even an expensive temperature-controlled crystal oscillator

has a stability of only 0.1 parts per million [50], which equates to a worst case gain or loss of around 8.6ms per day. Therefore, in order to be within the maximum permitted deviation of ± 10 ms from UTC, the system must be corrected once per day. This would be costly to do with telephone communications.

Practical alternatives to a clock based on a crystal oscillator are the radio time standards and the time information available from the global positioning system (GPS). Unfortunately New Zealand has moved to a digital radio transmission system, which has resulted in a slight, but random, delay as the signal propagates through a digital network, thus destroying the use of the once accurate radio timing pips. Furthermore, because remote installation sites and deployment outside New Zealand are a possibility, a solution based on the NZ radio time signals is unattractive. The GPS system offers significantly greater accuracy, as well as global coverage, and the continuing decrease in GPS receiver costs makes the initial outlay more affordable as well. For applications in urban environments, the use of a remote GPS antenna is required so that the receiver can have a clear view of the sky.

The design specifications for the recording system are therefore:

- 200 samples per second data processing and storage
- Highpass, lowpass, bandpass and allpass selectable digital filters on trigger data streams
- Greater than 108 kilobytes temporary pre event memory storage
- Greater than 4 megabytes of non-volatile data storage
- GPS timing system with remote antenna

5.4 User interface and communications parameters

Table 5 shows the desired parameters for the user interface and communications system as defined in the system requirements brief.

Table 5, User interface and communications parameters defined in the system requirements brief

Communications type	Wireless or telephony
Communications protocols	Preferable to use industry standards
User interface	Simple, intuitive interface structure Access to diagnostics information Access to stored data Access to configuration parameters

For the CUSP System to be interrogated or configured by a remote operator, some form of communications is required. The link between the instrument and the operator can be by physical cables or by radio channels. Installing cables between the central control point and each instrument in a network will be too expensive because of the need for large amounts of cable as well as a time-consuming installation process. The alternative option of using radio links does not provide the solution for all installation sites, as the wireless service may not cover the most remote instruments. In addition, both these schemes will suffer – to differing degrees – from interference, resulting in data loss or corruption.

These issues can be addressed by:

- Using existing communications facilities
- Mixing the transmission media (i.e. radio link then existing physical connections etc)
- Providing some form of error checking on data transmissions.

The best forms of existing wire connections are currently telephone networks and local/wide area networks (e.g. Ethernet and Internet). The use of the telephone network requires signal modulator/demodulators (modems) whereas the Ethernet requires network interface circuits.

The simplest data link between two points using the telephone network requires only the software routines to establish a connection. However, if the two communications points are separated across a toll-charge boundary, or the telephone network is charged on a time basis, this direct-connection method will suffer expensive network costs. In order to use the Ethernet network beyond direct connection of two points, the data transfer must be encapsulated by standard protocols that allow the network to direct the data to the correct destination. Thus, while the telephone and Ethernet networks provide a low-cost direct wire link between two points, in order to make the most effective use of them, adoption of standard protocols is required. The advantages of standard protocols include:

- Connecting through commercial communications providers (i.e. Internet service providers (ISPs)) resulting in low-cost telephone connections to local ISPs and then long-distance through the Internet.
- Increased reliability data transfer, for example by using the reliable 'transmission control protocol' over the 'Internet protocol' (TCP/IP)
- The possibility to include features such as email event alerts and automated record data transfer with TCP/IP
- Universal, low-cost remote connectivity.

For wireless applications, standard protocols can also prove beneficial, especially in terms of the increased reliability. It is even possible to use the same point-to-point protocol (PPP) used for telephone connections over cellular links. Standard TCP/IP is utilised for IEEE802.11 and the radio link protocol (RLP) can be used in place of PPP for radio modem links.

Standard protocols are not without disadvantages though. These include higher data processing loads and bloated data transfers due to protocol overheads. But even though a custom protocol ensures a minimal design, using standard protocols over

existing networks offers clear advantages provided the additional processing overheads can be tolerated. Furthermore, if the Internet protocols are provided, the resulting expansion in options for advanced communications can result in significantly improved functionality compared to contemporary instrumentation.

Transmission security is an issue when using public networks for data transfer. By providing data encryption layers, this can also be addressed by the use of standard protocols. For example, the 'secure sockets layer' (SSL) protocol, which is currently a 128-bit encryption scheme, offers (essentially) unbreakable data security.

Because of the advantages listed above, and since the processing facilities required are needed for both the data acquisition and the recording processes, the CUSP System is to adopt the use of standard protocols for data transfer, including the Internet protocol.

For an operator to communicate with an instrument, a simple and intuitive user interface is needed to prevent the operator from becoming confused when dealing with large numbers of instruments and from having to remember complex procedures if the system is not used frequently. Since standard Internet protocols are to be used for data transfer, a significant advantage would be to use standard software available on a typical personal computer as the interface. Such applications include the telnet and FTP clients and the web browser. Web browsers are the most desirable of these interfaces as they are widely used, provided with all major operating systems, can handle two-way file and data transfers and provide a familiar and intuitive graphical interface.

The design specifications for the communications and user interface are therefore:

- Connection through the public telephone network, Ethernet and via radio links such as IEEE802.11 and standard radio modems
- Standard communications protocols, such as PPP, RLP and TCP/IP providing assured reliability,
- Data security via encryption schemes
- Internet protocol allowing data transfer over the Internet.
- User interface provided by a web site.

Additional to these basic parameters, but desirable, would be the addition of automatic data management on a scheduled or event driven basis, such as:

- Scheduled (i.e. periodic) automatic generation and transferral of diagnostics (health) messages via FTP/SFTP or email etc.
- Automatic email of alerts when events occur (diagnostics or records)
- Automatic transferral of records to a central store after an event

The user interface must provide all the information and commands required to operate the CUSP System. Thus, many parameters must be viewable and adjustable. These parameters include:

- Configuration of the communications parameters of the CUSP System
- Configuration of the parameters controlling the data acquisition and recording processes (i.e. triggers, pre-event times etc.).
- View, download and delete records
- View, download and delete diagnostic reports
- View and delete diagnostics and web access logs
- Configuration of the web site, including item such as access rights to the website (security)
- Configuration of any scheduled or automated outputs of the instrument
- View the current status of the instrument

As the user interface is to be implemented as a web site, the issue of access security must be addressed. While the implementation of any security scheme is not discussed at this level, it is clear that some form of user differentiation should be provided to allow two levels of access: 'administrator' and 'general user'. This allows the configuration data to be protected from users permitted to view only information such as records, status and diagnostics.

It is advantageous to divide the information to be displayed or adjusted into separate pages containing related items. This prevents the user becoming 'lost' in data, simplifies the web page and also allows the development of the code generating the web pages to be modular and efficient. The anticipated pages required are grouped by functionality and access rights and are shown in Table 6.

Table 6, User access interface web pages

Page contents	Access rights
Data access, preview, delete etc	General user: read, preview Administrator: all
Read/delete diagnostics messages	General user: read Administrator: all
Read/delete website diagnostics messages	General user: read Administrator: all
Read/delete diagnostics reports	General user: read Administrator: all
Control security, control operation (logging etc) and configure display data (such as contact emails etc)	General user: none Administrator: all
Recording parameters, triggering parameters, instrument name etc.	General user: none Administrator: all
Internet parameters including modem and LAN settings	General user: none Administrator: all
Configuration of scheduled diagnostics messages, email alerts and automatic record transfer	General user: none Administrator: all

Sensor serial number, software revisions, time and GPS status, system voltage and temperature, storage space free, etc	General user: read Administrator: all plus trigger reset and manual trigger
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5.5 Physical parameters

The physical parameters that the system must conform to are shown in Table 7.

Table 7, Desired physical parameters for the CUSP System instrument

Case	Splash proof Withstand moderate physical abuse
Security	Lockable case
Power supply	Backup compatible
Temperature range	-10°C to +45°C ambient (operating)
Service lifetime	15-20 years

The physical parameters for the case present little design concern, but it must be considered a vital component of the system. A well-designed and specified case not only protects the components but also presents the instrument to the public. Furthermore, as this instrument is to measure ground acceleration, a direct and well-coupled physical connection to the mounting surface must be provided. The case must also be simple to operate, and provide good access to the components inside for inspection, repair, adjustment (if necessary) and access to any connectors etc.

Because the instrument may be installed at remote locations, the instrument must be capable of operating from a solar cell or other low voltage source. Furthermore, the use of mains power is to be avoided to minimise legal and regulatory obligations. These two considerations make it the obvious solution to power the system from a low voltage direct current source. This has the advantage of transferring the satisfaction of regulatory requirements for mains powered devices onto a specialist power-converter manufacturer when mains power is required. As solar power and battery combinations are a likely to be used in some cases, the input range of the system should be compatible with this. Therefore, the input voltage range is to be 10-24VDC. The power supply must also provide information relating to the health of the input power to aid remote diagnostics of faults.

The backup supply is also required to prevent loss of functionality or interruption of service when the primary power fails. This demands the provision of two power supply inputs, with seamless transfer from one to the other. As the backup scheme will almost certainly be implemented with batteries, some form of protection to prevent over-discharge must be provided. Furthermore, the power supply must provide protection for the instrument in the event of incorrect application of input power (over-voltage or under-voltage, reverse polarity etc.) and protection for the power supply in the event of an instrument fault.

The temperature range is a difficult consideration to design for. Using wide temperature range components significantly increases the component cost and also limits the range of available components. Because the lowest cost 'commercial grade' components have an operating temperature range wide enough (typically 0-70°C) but that does not cover the low end of the required range, a possible means of permitting their use is to consider the heating effect of the instrument when operational, as the consumed power is converted into heat. This decision presents a calculated risk to reliability. In practice, this risk was proven acceptable, as from measuring the self-heating effect of the final product, a conservative addition to the lower temperature limit for the system components is 10°C above the ambient temperature. Applying the 10°C self-heating allowance to the lower temperature limit shifts the instrument's operating temperature range into that of commercial grade components.

The design specifications for the physical parameters are then:

- High mechanical coupling of case to physical mounting point.
- Sealed, water resistant case.
- Tolerance to moderate physical abuse on case.
- Lockable case.
- Easy access to all required system components for inspection, replacement and adjustment.
- Operating temperature range of 0°C to +55°C inside case, -10°C to +45°C ambient.
- 10-24 volt input power range.
- Dual input to allow addition of backup supply, with selectable over-discharge protection scheme.
- Protection against incorrect power application/connection.
- Information must be provided on the health of the input power.
- A designed service lifetime of 15 to 20 years.

6 A new approach for low cost, complex and long lifetime instrumentation

6.1 Introduction

After reviewing previous work, described in chapter 4, two major problems are apparent with the traditional approach of using a custom processing platform with a custom operating system: 1) the reliance on specific hardware components and the design's consequent vulnerability to inevitable component obsolescence and 2) the high interdependence of the operating system to the specific hardware platform. These two problems are typically interrelated; hardware changes resulting from repairs or obsolescence may require the modification of the operating system and, functional upgrades are limited by the hardware. These two factors present a serious design problem if the desired long lifetime and upgradeability of the CUSP Instrument is to be achieved.

This chapter aims to address these issues. Because the CUSP System is complex and aims to provide a long service lifetime at a low cost, the chapter begins by making the terms low-cost, complex and long lifetime more precise. This is followed by a brief discussion of the problems experienced when trying to combine these three aspects, and is where the issues of component obsolescence and software maintenance are introduced.

A discussion on the issue of component obsolescence is given, showing that it is a serious issue for all long lifetime systems. Options that can be considered to mitigate this problem are discussed in general terms and summarised. Then, at the conclusion of this discussion, the issue of the operating system/system software is considered.

A new approach is then presented that, for products such as the CUSP System, provides an elegant solution. The solution is achieved by creating a high level design of low-cost, modular, and preferably commercial off-the-shelf (COTS) subsystems. When combined with a generic operating system and well-specified

module interfaces, this approach places the emphasis of the design at a much higher level than with the design of traditional high-performance datalogging equipment. This results in the flexibility to maintain or upgrade the design with minimal redesign or integration effort, using different, but largely equivalent, subsystem components. Therefore, though manufacturers or technologies, or both, may change, the manufacturers device drivers, combined with the standard hardware and software interfaces and the buffering function of the generic operating system, mean that the custom developed aspects of the system are protected from hardware changes.

A summary is then presented outlining the various benefits and limitations of this approach and a conclusion is made to its suitability for the CUSP System.

6.2 Definition of low-cost, complex and long lifetime instrumentation

Complex instrumentation systems are, for the purposes of this discussion, defined as systems requiring non-trivial data processing facilities and/or high bandwidth data gathering capabilities. The implementation of complex systems therefore requires highly-integrated⁷ components such as microprocessors. Typical examples could be a remotely configurable seismograph or an electrocardiograph machine.

Long lifetime systems are defined to have a service life of a period exceeding that of the mean-time-before-failure (MTBF) of the components making up the system. While it is not possible to give a limiting value here, this classification is to differentiate between products that are expected to require servicing during their lifetime (e.g. the bulk of medical, aerospace or military systems), as opposed to

⁷ A highly-integrated component is a component that is a conglomerate of sub-components, which together provide a specific functionality. An example is a 'radio-on-a-chip' that requires headphones, an antenna, a few buttons and a battery to make an entire radio, c.f. 10s or 100s of discrete component to achieve same result.

products that are either obsolete or uneconomical to repair by the time they fail (e.g. cellular phones).

Low-cost systems are defined as systems that are designed and constructed to meet a minimum build and sales cost, thus, the final cost does not include charges for any scheme to provide protection from obsolescence. This definition differentiates between products with a cost that reflects the costs of the constituent components, and products that have an additional cost that covers the manufacturers anticipated expenses to maintain the product for an extended product lifetime.

6.3 Long term design problem

The requirements of complexity, low cost and long lifetimes are mutually exclusive when considering component obsolescence: complex systems consist of large numbers of highly-integrated, difficult-to-substitute components; low-cost implies no redesign budget or allowance for maintaining component supplies beyond the construction period; long lifetime requires component replacement within the service lifetime of the system.

Further to the problem of producing a long-lifetime, low-cost and complex device is the almost certainty of such a device containing a processor system, and therefore, an operating system. The traditional custom operating system developed for a custom hardware platform exhibits close integration with the hardware to maximise efficiency and minimise development time, since the target functionality is well defined and its scope limited to a specific requirement. This close integration adds to the component obsolescence problem, as component changes or redesign work can result in the need for significant reprogramming of the operating system and application software.

6.4 Hardware component obsolescence mitigation

Electronic components originated with the invention of the electric lamp. Edison himself was the first to note, in 1880, the rectification effect of wires introduced into a lamp that eventually lead to the development of the thermionic diode, triode, pentode and other fancifully-named devices. Unfortunately the 'valves' (as they were called) were bulky, fragile, and required high voltages and currents to operate. The electrical properties of various solid-state alloys and substances were well known at this time, but until the discovery of the P-N junction by R.S. Ohl (around 1941) the practical results were limited to rectification (point contact diode etc.), even though photo and thermo sensitivities had been observed [53].

The first amplifying solid-state device produced was the transistor, developed by W.H. Brattain and J. Bardeen at Bell Laboratories in 1945. Manufacturing developments such as using diffusion and etching processes on the raw materials (silicon and germanium) resulted in the first integrated circuit in 1959, produced by J.S. Kilby, in which many transistors were contained in one solid piece of substrate [53].

Since the development of the first integrated circuit (I.C. or IC), devices have been made with increasing levels of complexity and specialisation. The measure of the complexity and specialisation is known as the 'integration level', with a more highly-integrated component providing more of the functions required to perform a certain task in one single device. Unfortunately, the increasing level of integration, and hence specialisation, of components means that as technology moves onwards, components are manufactured for periods sometimes as short as two to four years [54] with an estimated 2000 electronic components are withdrawn from the market per month [55].

Clearly then, component obsolescence is a major problem that must be faced when seeking to design products with a long lifetime [56]. Component obsolescence must even be considered when product production is expected to continue for an extended period, as components will often become obsolete even during the development process [54].

Drawing from Stogdill [54], Madisetti et al. [56], Condra et al. [57], Pecht et al. [58], Solomon [59], Phophet [55] and the experience gathered through the work presented in chapter 4, methods to mitigate the problem of component obsolescence include:

- Designing with currently available components, with a purchase of supplies to meet future construction and maintenance needs,
- Redesigning/substituting when required with new components
- The use of military specified components, with their guarantee of long availability, or with ‘garden variety’ components with their popularity increasing the likelihood of continued availability,
- Placing high-risk components on easily redesigned throwaway modules connected with standard interfaces,
- Observing industry investment in technologies and choosing components based on their likelihood of future availability

Each of these options has individual costs and benefits and will be discussed in the following sections.

6.4.1 Design with currently available components – the ‘lifetime buy’

This option presents the least initial design effort, and freedom of component selection resulting in an optimal and ‘minimum cost design’. This is due to the use of specialised components with high levels of integration. Highly integrated parts decrease component counts and costs, as well as reduce the end product’s size and power consumption. While these aspects are beneficial to producing low-cost, high-tech, throwaway products such as cellular phones or desktop PCs, these components are usually only supplied for as long as the targeted technology lasts, and the future substitution of such highly-integrated components is almost impossible.

Furthermore, this approach simply transfers the obsolescence costs from design to production/maintenance budgets by requiring the bulk purchase of all components with an obsolescence risk, thus maintaining a supply for future construction and maintenance purposes [54]. While this has a large initial expense, if the estimates of future requirements are accurate, this will not present undue expense in the long term. This commitment does, however, tie the design of the system to a particular technology, creating a technology snapshot, thus limiting the ability to capitalise on future innovations.

6.4.2 Redesign/substitute when required with new components

Redesigning the system to use substitute components, as maintenance requires, is perhaps the most risky option. Special effort must be applied to selecting a level of component integration that balances the design bloat of using too many simple devices against the difficulty in substituting an optimal, but highly integrated, component. It is also difficult to predict future trends in inter-component interfaces, standard supply voltages etc. Even if direct upgrade parts are available with the same functionality, form and voltages etc, differences in subtle parameters such as logic rise times may lead to downstream complications with integration and also affect factors such as electromagnetic interference approval etc. [55].

While this option may be initially cheaper than stocking large numbers of replacement parts, it may equally prove to be a near impossible task to substitute by redesign. Depending on the exact component requiring replacement, this approach may even require a complete system redesign. The approach does, however, allow some limited ability to capitalise on technology advances. Additional problems may be posed if the redesign involves modification of the operating system.

6.4.3 Use of military specified and/or 'garden variety' components

Components with a military specification are designed for ruggedness and reliability, driven by their critical function. Military applications, with a long product lifetime, require the extended availability of the components to allow continued support and replacement of failed parts. This technology has also been adopted by some commercial applications such as passenger aircraft, which may have a 20-year airframe lifetime.

However, as electronic component consumption in the commercial sector has steadily grown with consumers demanding greater technology in everyday devices, the military now represents just one percent of the electronic component market [54]. As a consequence of the reduced importance of the military market to manufacturers, the number of military qualified component manufacturers (QML certified) has dropped, resulting in concerns for the future availability of military components [58]. Furthermore, as the design and qualification process for military components is more stringent and expensive, the range of available technologies is limited and the components can cost as much as eight to ten times more than commercial grade components [58].

The use of military-specified components is therefore not only initially the most expensive option, but it may also result in a cumbersome design because a greater number of less-integrated components may be required than when using highly-integrated commercial grade components

The use of 'garden variety' components also suffers from the design bloat problem for the exact same reasons as the military components; many basic components are

required to meet the functionality of a single highly-integrated part. This also increases circuitry size and power consumption, both of which increase overall cost.

6.4.4 Designing high-risk components onto easily redesigned throwaway modules

Placing high-risk components on essentially ‘throwaway’ modules presents an elegant solution, but requires much more effort in the specification and design phases to ensure that the interfaces between modules will be compatible with predicted future trends. Defining the boundaries of the modules becomes an issue requiring careful consideration in order to balance the loss of hardware whilst maintaining the ability to replace vital components. For example, does one include system memory with the processor module or should it be contained in a separate module?

The biggest advantage of this approach is that provided standardised interfaces are chosen, the lifetime of the system can be increased because, in general, interfaces and architectures outlive many generations of individual components [60], as shown in Figure 10.

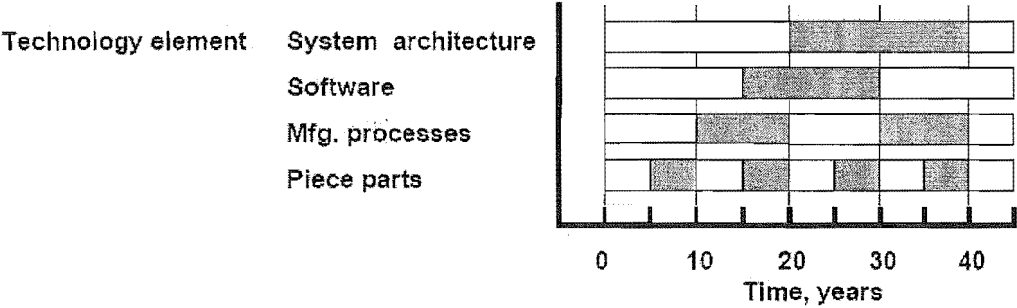


Figure 10, The lifetimes of system architectures relative to components (after Condra [60])

6.4.5 Observing industrial investment and choosing ‘safe’ technologies

As highlighted in section 6.4.3, the level of market demand for particular components or technologies is an important factor controlling the availability of components. The consideration of consumer trends can indicate likely areas of obsolescence as well as ‘safe’ technologies [59]. In the case of military components, with a small segment of the market, this has resulted in the continued reduction of availability; on the other hand, the heavy demand for, and investment in, the personal computer segment has caused the continued availability of backwards-compatible processor circuitry, even though the root technology is now obsolete. The x86 processor family is a good example of this.

This approach applies equally to standards such as interconnection buses and interfaces; by observing industrial or commercial investment in a standard, an estimate can be made to its likely future and therefore the safety in its adoption. Using accepted standards for interfaces within the system and as expansion ports helps ensure that the system can incorporate improved performance components in the future as well as potentially allowing original equipment manufacturers (OEMs) to supply system components, such as GPS receivers etc.

6.4.6 Use of COTS subsystems

COTS systems are essentially ‘black boxes’ produced by OEMs to perform a given task. By definition, COTS equipment is ‘off the shelf’, meaning the development costs of the product are not borne solely by a single consumer. Furthermore, all issues of individual component obsolescence are borne by the manufacturer of the COTS equipment, thus taking the obsolescence burden off the system integrator. The use of COTS items is widely regarded as being a ‘golden bullet’ for the problems of obsolescence management and has even become a preferred approach for the US military for minimising obsolescence [58].

The transfer of the component obsolescence burden back onto the COTS manufacturer does not, however, mean that a specific COTS item will remain available over a long period, unless some arrangement is made with the COTS manufacturer. This difficulty may be mitigated to a certain extent by using only generic COTS equipment, produced by many manufacturers and with a heavy industry investment, thus ensuring manufacturers are encouraged to produce at least functionally compatible products in the future. This has been the approach the Boeing Commercial Airplane Group has adopted for its avionics packages for commercial aircraft [57].

COTS equipment is especially attractive for low-volume applications; the mass-production of the equipment reduces the build costs, so that even with profit margins included, the selling price is something similar to the cost of a custom product made in low volumes. This results in a similar component cost but eliminates the development time and expense needed to design a similar, but custom, device.

6.5 Operating system / software issues

Two options exist for a systems software or operating system: custom or generic. In this case custom is defined as *an operating system developed specifically for the hardware system and target application under development* and generic as *an operating system developed for a standard hardware platform and generic applications* e.g. Windows, UNIX or DOS.

The custom option is usually developed for use solely on a specific platform. This allows it to be optimised for both speed and size. A smaller, higher performing operating system is beneficial for reducing both memory and processor performance requirements, which results in lower power requirements. The main disadvantage of a custom system is that it is labour-intensive to develop and even more so to maintain it to cope with modifications to both the system functionality and the hardware platform.

Generic operating systems require standard platforms (x86, ARM, PPC etc) but are often capable of operating on multiple platforms (for example Linux and Windows CE). They are not usually optimised for a particular task and consequently are usually much larger and slower than a custom operating system. Also, real-time operation is not usually provided. The advantage gained from this size increase is conformance to standards, particularly interfaces to hardware. Thus, as the product's custom software applications are buffered from the hardware platform by the operating system, portability is increased so the applications can easily be adapted to different hardware platforms. Because the operating system provides all the low-level functionality, such as file access and network communications, a further advantage is that programming effort and time are reduced.

6.6 Use of modular design approach with COTS technology components and generic operating systems

Of the design options presented above, the modular approach offers the best compromise between the conflicting parameters of design time, initial costs and, critically, maintenance costs. While a modular approach limits the scope of the effects of obsolescence to a module level, the overall the effect of obsolescence still results in considerable expense and effort. However, the use of COTS components for the system modules provides an elegant solution to this problem, provided that the COTS components have an assured availability lifetime exceeding that required of the resulting system.

While this pushes the obsolescence issues onto the COTS equipment manufacturers, this direct approach is unlikely to meet the low-cost criteria, as the costs to the manufacturers of assuring a long-term supply must be included in the cost of the COTS components. Therefore, in order to obtain a low overall cost, the system must make use of low-cost COTS equipment, and accept that the exact replacement component may not be available for the full lifetime of the product. Thus, the resulting system must be capable of adapting to replacement COTS equipment with differing technologies and performance levels.

The design's ability to adapt to different, but functionally similar, COTS devices can be achieved by a combination of using standardised inter-module interfaces with a high level of commercial and industrial investment, combined with a generic type operating system for processor based modules. Thus, even though replacement COTS modules may have different performance levels or operate in a slightly different way, the integration can be assured because the new device's hardware looks identical through the inter-module interfaces, and for processor based modules, the operating system performs the low-level functions, thus buffering the product's custom software from the potentially different hardware platform.

The use of standard interfaces has the further advantage of the possibility of adapting the design to technologies not available at the design time. For example, in a system containing a COTS processor core, it may be possible to move from wired to wireless communications simply by the connection of a wireless network device to a standard port and adding a new device driver to the operating system.

Some modules will be either too specialised or too trivial to use a COTS device. However, standardised interfaces should still be used to ease potential future modifications. Furthermore, to maximise the advantages of the reduced design effort and the lowered obsolescence concerns, careful consideration should be given to the option of using an over-specified COTS component in place of a directly realisable, but relatively complex, custom module, even though the COTS device may use more power or contain redundant features.

Several disadvantages with using this approach must be recognised. When externally supplied components are sourced, the system is now exposed to external sources of design error or manufacturing flaws. These are generally not repairable or modifiable by the developer and must be factored in to the overall design cost and time budget. Generic operating systems may introduce potential security breaches, depending on the application, and, like all software, may contain software bugs resulting in poor or undesirable operation.

Another serious design issue is the generality of function when limited to COTS devices. This may result in built-in over-design, with many unused and unwanted

features. These will increase the power consumption and susceptibility to system failure, which is related to the component count. However, the costs of an over-designed system may be offset by the decreased design time and cost, reduced obsolescence concerns and the lower module costs due to the use of mass-produced COTS components.

6.7 Conclusions

The approach described in this chapter provides an effective solution to the long-term design problem when considering development, build and maintenance efforts and costs for this type of application.

The approach maximises upwards compatibility and permits redeployment with new performance standards by virtue of the adoption of industry-supported interface standards and the large range of specialised components that are available which use these interfaces. The individual component obsolescence problem is pushed back onto the COTS manufacturers in the short-term, and in the long-term, the designer/maintainer has only to contend with interface and systems architecture obsolescence, a more manageable proposition. Design obsolescence is further minimised when using industry-standard modules, since the large investment ensures continued supply of functionally compatible components in one form or other.

A disadvantage of the approach is the risk of unused functionality bloating the design and increasing the power consumption due to the possibility that the COTS components available do not exactly match the requirements – it is almost certain that a COTS component that meets the minimum requirements over all areas will exceed them in some. A further disadvantage when using a generic operating system is the risk of system exposure due to software security issues. The security risks can be minimised by using up-to-date security patches as well as by ensuring careful deployment e.g. minimising visibility of unit on public networks. There is also the risk of hardware faults in COTS components. This can be rectified by either return to the manufacturer, or by replacement of the component with a compatible unit. This is

an implicit risk in all designs but in this case the fault cannot usually be rectified locally, due to a likely lack of service information on the outsourced design.

In general, this approach offers the best compromise for the long-term, low-cost design problem for the CUSP System and other similar complex, low-cost equipment requiring a long service lifetime.

7 The definition of the system subsystems, approaches to realise them and the consequent design map

7.1 Definition of the CUSP System subsystems

With the design of any system, the identification of the systems components or subsystems is an important process, permitting the design to be divided into manageable sections. For this project, with its goal of minimising obsolescence issues (chapter 6), the module boundaries and interfaces require clear definition, since at the end of the products life cycle the interfaces may be the only recognisable components of the original design.

Because some of an individual subsystem's hardware may be controlled by software routines operating on another subsystem, boundaries between subsystems may be blurred. In order to define these boundaries more clearly for design and specification, those software components that are not directly linked to a particular subsystem's hardware (e.g. a microprocessor controlled data acquisition system), should be contained in a generalised software subsystem.

Considering the above point, and using the results from chapter 5, the development of the design specification, the CUSP System can be broken into the obvious distinct subsystems described in the following sections.

7.1.1 Central processing subsystem and operating system

A processing platform is needed to provide the data processing requirements of the recording and data processing software routines. This subsystem includes a hardware system and a software-operating environment to allow execution of the necessary software routines, as well as hardware to store data and programs. The software operating environment, or operating system, includes application management, device

drivers, file management and network stacks etc. This subsystem has been named the *central processing subsystem*. The description above, combined with the relevant tasks listed in the design specification (chapter 5), are summarised in Table 8.

Table 8, Central processing subsystem components and functions

Hardware components	Software components
Processor hardware platform	Operating system
Data storage hardware	Communications facilities / servers etc
Data acquisition subsystem interface hardware	Security / encryption schemes
Power supply subsystem interface	
Communications subsystem interface	

7.1.2 Data acquisition subsystem

The data acquisition hardware specification presents clear subsystem boundaries by virtue of the requirement for the data acquisition system to be upgradeable and self contained. While a hardware boundary can be drawn around the data acquisition circuitry and the interface to the processing platform, the software boundary is less clearly defined, as discussed in section 5.2. Thus, the data acquisition subsystem boundary will enclose the translation of seismic signals to the digital domain, the correction of transducer errors and the transferral of this data to the central processing subsystem for further signal processing. This has been named the *data acquisition subsystem*. Combining the above discussion with the relevant tasks listed in the design specification given in chapter 5, results in the summary given in Table 9.

Table 9, Data acquisition subsystem components and functions

Hardware components	Software components
Transducer hardware	Data sampling
Antialias filter hardware	Correction of transducer errors
Analogue to digital conversion hardware	
Sampling and correction processing hardware	
Data processing interface hardware	

7.1.3 Time signal generation subsystem

The time information system comprises another subsystem. The separation of this function from the recording requirements enforces a specific interface specification to the time signal generating hardware, resulting in improved design robustness as per the approach defined in chapter 6. This has been named the *time signal generation subsystem*, and its components and functions are summarised in Table 10 after combining the above discussion and the relevant tasks listed in the design specification (chapter 5).

Table 10, Time signal generation subsystem components and functions

Hardware components	Software components
GPS receiver interface hardware	
Data processing interface hardware	

7.1.4 Communications hardware subsystem

Because communications technology is one of the most dynamic technologies the CUSP System uses, the communications hardware system is divided into a separate subsystem to ensure a specific definition of the interfaces between the subsystems for the same reasons as given above for the time signal generation subsystem. This module is termed the *communications hardware subsystem*. Adding the relevant tasks listed in the design specification (chapter 5) to the above discussion results in the summary presented in Table 11.

Table 11, Communications hardware subsystem components and functions

Hardware components	Software components
Data processing interface hardware	
Communications protocol conversion hardware	
Communications channel interface hardware	

7.1.5 Power supply subsystem

The power supply constitutes a clearly defined subsystem that provides power to the other subsystems. This subsystem must provide protection for the power source as well as the CUSP System, provide information on the health of the power source and supply power that meets the demands of the remainder of the system. This subsystem’s hardware must therefore be designed late in the design cycle, once the instrument’s power requirements are determined. This is called the *power supply subsystem*. Combining the above with the relevant tasks listed in the design specification (chapter 5), gives the summary presented in Table 12.

Table 12, Power supply subsystem components and functions

Hardware components	Software components
Protection hardware	
Voltage regulation hardware	
Power supply control hardware	
Data processing interface hardware	

7.1.6 Software suite subsystem

The software applications to perform the custom tasks specific to the CUSP System are collectively named the *software suite subsystem*. The software suite subsystem is to be modular (i.e. made of many separate components/applications) to ensure efficient design and to minimise the effects on other components of the software suite subsystem if a specific component requires modification. In particular, and to ensure that the portability benefits of using a generic operating system are preserved, any software closely linked to hardware must be kept isolated to reduce the consequences of any changes to the hardware systems.

Because a generic operating system uses built-in device drivers for standard devices, and also provides basic connectivity features such as modem control, TCP/IP stacks and FTP clients/servers, much of the basic low-level functionality is therefore already provided. The tasks then required of the software suite subsystem are listed in Table 13. Also shown is any hardware that each functional requirement is associated with.

Table 13, Required functionality of the software suite subsystem

Functionality	Linked to hardware components
Real-time collection of samples from data acquisition subsystem	Data acquisition subsystem
Real-time reading of GPS time information and processing	Time signal generation subsystem
Post sample processing of seismic data and detecting and recording events.	-
Overall command and coordination of the CUSP System	-
Monitoring of storage space available for records	- (Uses OS file system drivers)
Monitoring / controlling the power supply	Power supply subsystem
User interface	- (Uses OS webserver)
Email alert generation	- (Uses OS SMTP client)
Automatic record transfer	- (Uses OS ftp facility)

Diagnostic report generation and transfer	- (Uses OS ftp and scheduler facility)
Data output streaming over communications channels	- (Uses OS hardware device driver)

7.2 Approach taken for the CUSP system

This section outlines the approaches for implementing the functions and features defined in the design specification developed in chapter 5, in terms of the subsystem boundaries defined in the previous sections. It also defines the inter-subsystem interfaces. The approaches chosen must also ensure the resulting instrument meets the constraints of both low-cost and maintaining a 15-20 year service lifetime by following the approach outlined in chapter 6.

7.2.1 General approach

Because the specification of some of the subsystems depends on others, the order of development is not arbitrary. The central processor subsystem is discussed first since it is the core of the design, because it contains the highest-level task of control and coordination of the instrument. The power supply is presented last, as this must meet the demands of the other subsystems.

7.2.2 Standard interfaces

As discussed in chapter 6, the choices of standard interfaces are, in conjunction with the choice of generic operating system, the most critical design choices that must be made for the implementation of the CUSP Instrument due to their importance to the longevity of the product. Interfaces that lose popularity or support will have a negative impact on the range of replacement COTS modules available in the future.

To this end, the interfaces chosen are limited to standards that currently have strong industrial and/or commercial support. The choice of interfaces within this subset must be further narrowed to the selection of those that are either so ubiquitous as to ensure ongoing support, or that provide a clear upgrade path, which maximises the likely longevity of the interface. Furthermore, interfaces for aspects of the instrument that are likely to require additional bandwidth in the future, such as data acquisition modules, should have an expandable data transfer capability, such as serial interfaces.

Amongst the more popular interfaces are the types supported by the industrial and home computer industries. Their use widens the range of supported COTS modules, from modems to uninterruptible power supplies. A brief summary of some of these interfaces are given in Table 14 (after [61] [62]).

Table 14, Popular commercial and industrial interfaces

Standard	Data width	Notes
RS232	Serial	Real-time signalling but async data transfer
RS422/485	Serial	Real-time signalling but async data transfer
IEEE-488 (GPIB)	8	Instrumentation standard
VME	8/16/24/32	General purpose industrial interface
PC parallel port	8	Generic PC 8-bit digital input, 4-bit output
PC serial port	Serial	Real-time signalling but async data transfer
SCSI	8	High-speed used mainly for hard disks
USB1.0	Serial	Not real-time
USB2	Serial	Not real-time

IEEE-1394 (Firewire)	Serial	Not real-time
ATA/66	16	High-speed used mainly for hard disks
ISA	16	Outdated PC bus
PC104	16	Current industrial version of ISA
PCI	32/64	Standard PC bus

The actual choices of interfaces for the various subsystems will be, to a large extent, driven by the central core of the instrument, which, as discussed in section 7.2.1, is the central processor subsystem. This is because the architecture of the chosen processing platform hardware will be optimised for particular a suite of interfaces for input and output. Furthermore, a generic operating system will provide greater support for the more common interfaces.

7.2.3 Central processing subsystem

7.2.3.1 Hardware

The central processor subsystem hardware is the physical platform that contains the processing circuits and hardware peripherals to support the operation of the operating system. The peripherals include such items as program memory, expansion busses and record storage memory. To design a processing platform that meets the long lifetime goal whilst avoiding obsolescence and retaining a low cost is a difficult problem due to the complexity of the required circuitry. As discussed in section 6.6, COTS equipment with technologies, interfaces and operating systems that have strong industrial support represents the lowest risk solution for complex system components. Therefore, for the CUSP System, a COTS single board computer (SBC) provides the best option for providing the required processing functionality. Of the available

processing platforms (MIPS, ARM, PowerPC etc.), a COTS x86 platform was chosen for a number of reasons:

- Mass production, therefore very low cost; for example, they offer much more processing power and features than the DSP-based prototype instrument yet have less than half its construction cost.
- Widespread commercial use, therefore a large support base and range of manufacturers. A further advantage is that the existing investment in this technology essentially future-proofs it, even if a future replacement module is of a different architecture that emulates the x86 processing platform.
- Available in low power versions for remote sites.
- Generic operating systems are available, reducing software development time and effort, as well as increasing maintainability.
- Standardised functionality is maintained across manufacturers, and any slight differences can be buffered by a generic operating system.
- Has a wide range of cheap, mass-produced peripherals for communications and additional functionality.
- Standardised interfaces to other hardware using system buses (PCI, ISA, PC104 etc.), parallel and serial data ports (mouse, printer etc.) and IDE storage devices (hard disk and compact flash etc.).

The storage hardware should use solid-state media, to provide reliable operation in rugged conditions and to ensure optimum power efficiency. As many SBCs are available with compact flash ports, or at least IDE drive interfaces, the use of compact flash is desired because it is a cheap, reliable and widely supported technology.

x86 SBCs offer a wide range of interfaces allowing expansion; the interfaces common to almost all SBCs include PC104 or ISA busses, serial communications ports and the parallel printer port. Many SBCs also include dedicated digital I/O interfaces, USB ports and built-in Ethernet ports.

7.2.3.2 Operating system

The operating system is critical to the central processing subsystem, performing the hardware dependant low-level tasks and providing a stable operating environment that supports, amongst others, communications and storage facilities. It must be capable of operating fast enough to maintain synchronisation with the data acquisition and time synchronisation processes. In practice this necessitates near or fully real-time operation. The operating system should:

- Perform low-level tasks such as driver initialisation, file system operation etc.
- Provide secure communications routines
- Provide data storage facilities (file systems)
- Communicate with/control a diverse range of hardware components
- Maintain synchronisation with incoming data and timing
- Support the operation of the CUSP specific software routines

The x86 hardware system has the ability to run generic operating systems such as:

- Custom operating system
- Microsoft DOS
- Microsoft Windows
- Microsoft CE
- Linux
- UNIX

The virtues and disadvantages of each will be discussed in the following sections.

7.2.3.2.1 Custom operating system

This requires the most development work of the six options, but results in a lean operating system that performs the required tasks at the highest level of performance, with real-time operation guaranteed. On the other hand, maintenance difficulties arise from the hard coding of drivers to access hardware features such as networking components and the communications protocols, as observed in section 4.4. Therefore significant work is needed to make even slight changes in the hardware parameters,

which effectively negates the advantage of using a 'standard' SBC, which appear identical to the product's custom applications when buffered by a generic operating system that uses manufacturer-supplied drivers. While there is no initial purchase costs with a custom system, due to the low-cost and long-term constraints on the CUSP System, development and maintenance costs make this an unattractive option.

7.2.3.2.2 Microsoft DOS

DOS provides the basic functionality to access storage media, provides system timing and offers the developer a base to work from. Real-time performance is usually possible but some hardware drivers can interrupt this, forcing the development of drivers for specific hardware on a device-by-device basis, as observed in section 4.4. This involves testing for individual hardware changes and may result in unpredictable behaviour. Thus, while DOS shortcuts much of the mundane hardware interfacing, the system requires extensive work for new hardware configurations. A further consideration is the licensing of the software, which has an uncertain future and may require the purchase of licences for the entire Windows suite to use just the DOS component. Therefore, even neglecting the maintenance efforts required, the uncertainty of long-term support eliminates this option.

7.2.3.2.3 Microsoft Windows

Microsoft Windows offers no real-time performance. A further disadvantage is the lack of scalability⁸ resulting in a rather massive and inefficient minimum installation. Network security is also an issue that affects Microsoft products to varying degrees and creates much additional work to maintain security. Furthermore, while Windows is continually upgraded, licence costs apply to each revision and it is therefore an expensive option. These disadvantages of Windows outweigh the continued upgrades available and the rich support for hardware devices and communications protocols.

⁸ Scalability is the ability to scale the size of the software installation to the intended application: in a scalable system, a simple system equates to a small install size.

Consequently Windows does not meet the low-cost and performance constraints and is eliminated.

7.2.3.2.4 Microsoft Windows CE

Windows CE provides the real-time components missing in Windows and also can be optimised for small install footprints. Windows CE provides most of the functionality required by the CUSP System but lacks certain communications facilities such as web servers or the PPP protocol in the basic form. Windows CE is part of the Microsoft suite and is therefore a strongly commercial product designed with a limited lifetime to force the user to upgrade to gain updated functionality. Security from network attacks is an ongoing issue that Microsoft has yet to resolve, creating much maintenance work to provide continued protection. These issues, combined with high licensing costs, outweigh the advantages of the high levels of support for various technologies. This option is also eliminated on the low-cost constraint.

7.2.3.2.5 Linux

Linux is a UNIX like operating system developed by Linus Torvalds and maintained by an open network of developers. Linux is released under the 'GNU Public Licence agreement' [63], essentially meaning the system is 'open source', allowing any user to develop specific modifications. Installations of the Linux operating system are diverse, with many slight variations. This allows the installation of a variant targeted specifically at the intended application, but also creates confusion with software version control. All additional applications for non-mainstream systems are (generally) required to be compiled by the user on their specific platform. A vanilla Linux installation may be created also by compiling the entire set of operating system components.

As Linux is released under the GNU licence, no fees or royalties are demanded, and, provided the user does not modify and release a Linux system, custom source code does not have to be provided to the general public or included with an embedded system.

Linux offers a high level of support for differing processor platforms⁹ and unlike Microsoft products is continuously upwards upgradeable without having to change the basic system. This permits upgrading without changing any custom applications or configuration settings, resulting in a simple and effective means to maintain compatibility with future developments.

The Linux kernel can be modified to run in a full real-time mode, providing guaranteed performance. Additionally, the high scalability of the Linux system means it can be built using the minimum required components, resulting in a very small deployment package.

The advantages of using Linux outweigh the initial difficulties in developing the system and provide confidence in the continued maintenance and ability to follow trends and upgrades in the hardware system.

7.2.3.2.6 *UNIX*

As Linux offers all the features of UNIX, as well as a more diverse range of supported targets and costs nothing, UNIX is discounted as a potential operating system.

⁹ E.g. ARM, MIPS, x86...

7.2.3.2.7 *Operating system choice*

It is clear that for the intended application, Linux offers the best performance with respect to scalability, cost, real-time operation and support for differing platforms. The slight reduction in availability of drivers for devices under Linux¹⁰ is not considered a hindrance for the CUSP instrument, as devices can be chosen that are supported by Linux.

The application of the Finite State Machines Laboratories Incorporated 'RTLinux' real-time kernel modification for Linux allows the operating system to realise the real-time requirements of the data acquisition subsystem and the GPS record timing interface whilst still allowing full access to the benefits of the Linux operating system.

7.2.4 **Data acquisition subsystem**

The data acquisition subsystem must acquire a digital representation of the motion of the earth, correct any errors arising from the acquisition process and transfer the data to the software suite subsystem via the central processor subsystem. While the digitisation process is straightforward, the correction process can be performed either in the analogue domain by hardware techniques or in the digital domain by software routines. Hardware based correction schemes will involve either complex analogue circuitry that may affect the gain and phase response of the system, or high power temperature stabilising systems, and thus it would be desirable to avoid them. Furthermore, hardware correction systems are likely to suffer from component temperature and aging effects. Software correction schemes, performed after conversion to a digital signal, are both easier and cheaper to implement, and offer the advantage of repeatability and stability without affecting the analogue signal.

Because no COTS components are available that fulfil the requirements of the data acquisition subsystem, a custom module is needed that contains a processor to

¹⁰ Most 'brand-name' components offer Linux support and drivers

coordinate the sampling process and to correct for the MEMS sensors errors. This subsystem will therefore contain circuitry prone to obsolescence problems. However, as the bulk of the high-performance data processing for the digital filters is to be performed in the central processor subsystem (section 5.2), the processor dedicated to the data acquisition subsystem can therefore be a low-cost microprocessor.

Because the most expensive components of the data acquisition subsystems are expected to be the acceleration transducers and the microprocessors, and as the transducers are to be upgradeable, the approach taken to avoid obsolescence issues in the data acquisition subsystem is to consider the entire subsystem as a throwaway module. As a throwaway item, the design process is permitted free choice of low-cost, highly-integrated and therefore high-risk components to produce a circuit with a minimum build cost and component count.

To provide for future upgrades of this subsystem, an expandable and long-lifetime interface is required. As the central processor subsystem is based on the x86 processor platform, the most appropriate means of interfacing with it is by the serial communications port. Due to the hardware configuration of the serial port circuitry, this port allows real-time signalling of data transfers (interrupt based) and by virtue of its serial operation, its use permits variable-width data transfers to cater for future resolution enhancements. Serial communication is possible over a number of protocols, including the robust RS422 format, allowing long runs of inexpensive cable between the data acquisition subsystem and the central processor subsystem. Furthermore, high-speed serial ports are also available, allowing up to 1Mbit/s of bi-directional data transfer, thus providing scope for future enhancements in signal handling capacity. Therefore, serial communications using RS232 or RS422 protocols has been adopted for this interface.

7.2.5 Time signal generation subsystem

The use of the time information contained in the GPS signal provides extremely accurate timing at a low cost, removing the major design concerns of trying to avoid the temperature fluctuations and component aging effects that plague free-running timing systems. However, the reception of the GPS signals at all times is not guaranteed. Factors such as foliage cover and urban shadow can block the signals sufficiently so that synchronisation is lost for certain satellite orientations. While this can be mitigated by careful antenna placement, consideration must be made for times when reception is lost, or times before GPS lock has been established, such as at instrument boot-up time. For these cases, the time signal generation subsystem must contain a local clock in addition to the GPS receiver.

For the CUSP System, the use of the standard x86 SBC platform provides the system with an inbuilt real-time clock (RTC). The accuracy of a generic SBC clock is not usually specified, but a conservative estimate would result in an error of around $\pm 30\text{ppm}$ [64], that of a standard quartz crystal. A $\pm 10\text{ms}$ error would therefore take just over 5.5 hours to accumulate, which represents the limiting period of acceptable GPS signal loss. This period will clearly be exceeded during times when the instrument is switched off, but GPS lock is typically re-established within 5 minutes of switch-on. The use of the SBCs RTC is thus considered an acceptable solution for backup timing, provided the instrument is installed with reliable power and good GPS signal reception (i.e. installed properly).

A stand-alone COTS receiver module, using NMEA communications, is the preferred option for the GPS receiver. This presents the design with a low-cost standardised ‘black box’, thus meeting the modularity and long-term availability goals. A further advantage of using the GPS system is the ability to extract relatively accurate positional data, which is useful for recording the instruments location as part of each event record.

The interface to the central processing subsystem is to a the serial communications port for the same reasons presented for the data acquisition subsystem. The use of the

robust RS422 communications protocol is particularly useful in this instance, allowing the receiver to be located remotely to provide optimal reception.

7.2.6 Communications hardware subsystem

The communications interface hardware is specified to use Ethernet, modem and wireless communications. The use of the standard SBC solution with a generic operating system for the central processor subsystem allows the communications hardware subsystem to be implemented with any of a wide range of standard components from USB wireless LAN to serial communications port telephone modems. This allows the communications hardware subsystem to meet the required long-term maintenance requirement by simply changing a failed device to another compatible device (along with its software drivers).

As most SBCs contain an inbuilt Ethernet port, this interface will be used as the primary interface. This provides high-speed communications between the CUSP System and a standard computer (including laptops) for configuration and software maintenance, and by configuring the Ethernet interface to masquerade with more than a single IP address, allows it to also function as a globally accessible connection. For SBCs with no built-in Ethernet port, this functionality can be provided with a standard PC104 bus Ethernet interface card or, for example, via a USB-to-Ethernet adapter.

In order to communicate over telephone or wireless channels, a serial communications port can be used with a COTS cellular, telephone or radio modem. High-speed short-haul wireless communications, for array networking, can be achieved with the IEEE802.11 standard devices attached to the SBC's USB, compact flash or PC104 interfaces.

7.2.7 Power supply subsystem

In order to simplify the design of the power supply, reduce the construction costs and to provide a standardised configuration for differing applications and countries of use, the power supply is to be powered from low-voltage direct current (D.C.) sources. If the instrument is required to operate from mains power, the system installer can source locally approved COTS power converters. This is expected to provide a worthwhile reduction in overall cost due to two factors:

- Many instruments will be deployed at existing seismograph sites that already have D.C. supplies,
- It is impossible to compete with COTS manufacturers when making low-volume products, especially when considering the safety certification process.

For the same reasons, no battery charging circuits are provided, either. This frees the system installer to choose battery capacities optimised for their application and to employ locally sourced and approved chargers. While it is traditional to include a battery and charger with a strong motion instrument, by not including them, the selling price of the instrument can be kept low. Local, off-the-shelf equipment will cost the installer no more than if they were supplied with the instrument, and will comply with local regulations.

The power supply subsystem must provide power for the other subsystems comprising the CUSP System, but the exact output requirements can only be determined once the other subsystems are designed/developed. However, the input parameters are better known. The input to the system is specified as a direct current of variable voltage. Input from a backup system must also be catered for and protection from over-discharge of a backup battery should be provided. Protection must also be provided for both the power source from system faults and for the system from incorrect source application.

The requirement for over-discharge protection for the backup supply presents a design issue that demands communication between the power supply subsystem and the central processor subsystem. This allows the CUSP System's software to test the

backup system's voltage, and to set in motion the orderly shutdown of the instrument when a low battery condition is detected (and only when no events are in progress). Therefore, a communications interface must be defined. The monitoring of the supply health and the corresponding control response of the power supply subsystem requires a bi-directional communications interface, and since the signalling can be digital, one of the SBC's digital interfaces can be used. In order to maintain maximum flexibility and standardisation between differing SBCs, the parallel printer port is chosen for this task because it offers standardised bi-directional digital signalling with multiple I/O lines and simple hardware addressing.

The variable D.C. input requires regulation in order to be applied to the other subsystems. To maximise efficiency, switching regulators are the only practicable solution.

The requirements for switching regulators, combined with supply monitoring and power supply control over the parallel printer port, results in a subsystem that is unlikely to be available off-the-shelf; thus, a custom design is required. The complexity of this subsystem results in the most risky design aspect of the CUSP System in terms of long-term maintenance. The complex nature of switching regulators and their typical dependency on identical replacement parts requires that this subsystem be designed with a combination of life-time-buying of parts and a threshold past which the design is abandoned, and a new subsystem designed. While this is not optimally cost effective, the design should aim to use garden-variety parts where possible. Since the efficiencies of SBCs and switching regulator circuits are increasing with time, the supply's output requirements will change; therefore, the inconvenience of periodic redesign is offset by the benefit that it ensures the subsystem maintains optimal performance.

7.2.8 Software suite subsystem

The software suite subsystem controls the coordination and operation of the entire CUSP System. As discussed in section 7.1.6, the primary concern is for maintaining modularity to prevent the system becoming difficult to adapt to any future changes in hardware i.e. maximising maintainability. It is imperative then that careful attention is paid to the breaking down of tasks into separate components. Of the options taken to realise this, the simplest and most effective is to completely sever the tasks into specific functions and allow them to communicate via external interfaces such as shared memory segments, semaphores and via configuration and data files. The adoption of a daemon¹¹ approach for many tasks ensures efficient processor usage and further helps to maintain modularity.

The breaking down of these tasks is discussed in chapter 9, which outlines the design of the software suite subsystem components.

7.3 System design map

A graphical sketch of the basic system, as defined in the previous sections, is shown in Figure 11. This indicates the hardware boundaries and interfaces between the basic components of the CUSP Systems subsystems.

¹¹ An application that sleeps in the background while waiting for a particular event to occur, activates when the event occurs and performs its programmed task, and then returns to the background.

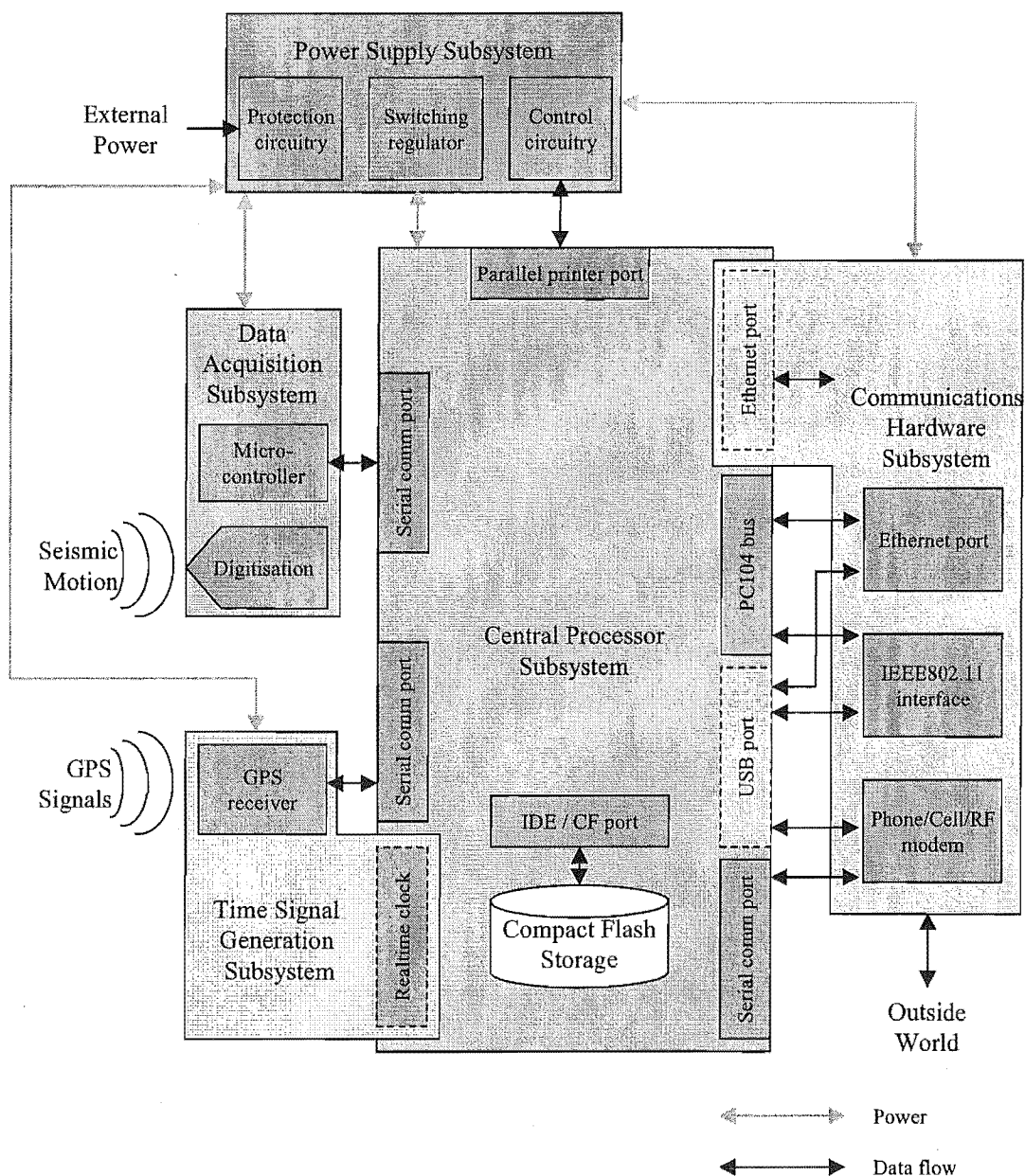


Figure 11, Sketch of the basic CUSP System subsystems and interfaces

8 Characterisation and correction of MEMS accelerometer response

8.1 Introduction

This chapter discusses one of the major issues this thesis addresses; the characterisation and correction of the errors that the MEMS accelerometers exhibit. The chapter begins with a review of classic accelerometer theory, and then discusses, in broad terms, the effects of adding feedback to an accelerometer.

Because the constraints of cost and availability limit the choice of sensor for the CUSP System to just one device, the sensor is specified at this point. The characterisation of the device is then presented, providing detailed information on the type and magnitude of any errors.

A discussion on various techniques that can be employed to remove these errors is made, and the various techniques tested. The results of these tests are presented and a choice is made on the best approach for correcting the errors of the CUSP System's sensors.

8.2 Classic accelerometer theory

Drawing from Bullen and Bolt's text: 'An introduction to the theory of seismology' [5], a classic sprung mass pendulum has the basic construction shown in Figure 12. The three forces that act on the mass in absence of any external excitation are the spring force, F_S , the inertial force on the mass, F_M and the damping force, F_D .

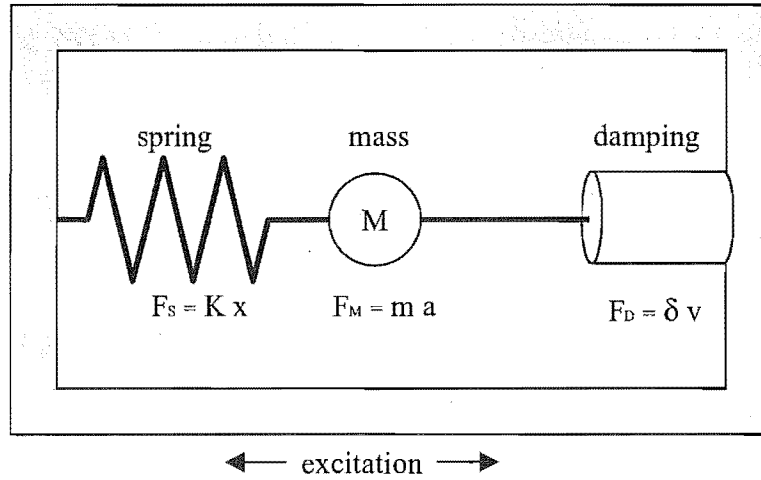


Figure 12, Basic construction of a spring mass pendulum

All the forces must equate to zero in a static system, thus:

$$F_S + F_D + F_M = 0 \quad 1$$

Writing this as a function of time, with δ being the damping factor proportional to the velocity, m being the mass of the pendulum and K being the spring constant we have:

$$m\ddot{x}(t) + \delta\dot{x}(t) + Kx(t) = 0 \quad 2$$

Dividing through by the mass, and rearranging we get:

$$\ddot{x}(t) + \lambda\omega_0\dot{x}(t) + \omega_0^2x(t) = 0 \quad 3$$

Where $\omega_0 = \sqrt{\frac{K}{m}}$ and $\lambda = \frac{\delta}{2\sqrt{Km}}$. ω_0 is referred to as the natural or resonant frequency of the pendulum system.

When an external excitation is applied, the applied acceleration must be added to the mass force term so that in effect we have:

$$\ddot{x}(t) + \lambda\omega_0\dot{x}(t) + \omega_0^2x(t) = -\ddot{u}(t) \quad 4$$

If the applied acceleration is periodic, $u(t)$ can be written as:

$$u(t) = A\sin(\omega_A t) \quad 5$$

Where ω_A is the applied signals frequency, and A is the amplitude. The differential then becomes

$$\ddot{u}(t) = -\omega_A^2 A\sin(\omega_A t) \quad 6$$

Thus

$$\ddot{x}(t) + \lambda\omega_0\dot{x}(t) + \omega_0^2x(t) = \omega_A^2 A\sin(\omega_A t) \quad 7$$

The solution to this is rather complex but the essential form for the magnitude response is:

$$x(\omega_A) = \frac{A\omega_A^2}{\sqrt{(\omega_A^2 - \omega_0^2)^2 + 4\omega_A^2\omega_0^2\lambda^2}} \quad 8$$

Which shows the critical dependence on the damping factor λ . As λ approaches zero, $x(\omega_A)$ reaches asymptotic values when the applied frequency matches the resonant frequency. Generally designers aim for a damping factor from $1/\sqrt{2} \leq \lambda \leq 1$, where $\lambda = 1$ is critical damping [5].

It should be noted that from the spectral response (equation 8), that the output is not constant for all frequencies of excitation. When the primary input signal is well below the natural frequency of the pendulum, and neglecting the damping terms, equation 4 becomes:

$$\omega_0^2 x(t) = -\ddot{u}(t) \quad 9$$

This implies that the output of the pendulum system will be proportional to the acceleration of the input signal. Conversely, if the input signal is at a much higher frequency than the resonant frequency, equation 4 simplifies to:

$$\ddot{x}(t) = -\ddot{u}(t) \quad 10$$

Equation 10 indicates that the pendulum now responds to the displacement of the pendulum system. Thus, equations 9 and 10 show that the selection of the resonant frequency of the pendulum and the damping factor determines the output response of the classic pendulum.

8.3 Feedback accelerometers

The introduction of a force feedback loop (servo response) into the classic pendulum system has the equivalent effect of removing the damping term from the equation of motion of the pendulum system so that the dominance of the $Kx(t)$ term of equation 2 results in a nearly ideal accelerometer. In practice, the natural frequency increase is limited because of both the loop gain of the feedback loop falling with increasing frequency, and the limitations of the force feedback mechanism. However, the performance of feedback-controlled pendulums used as accelerometers is significantly better than the classic pendulum for seismic analysis purposes.

8.4 Micromachined accelerometers in the CUSP System

The maturing of micromachining technology to mass-production processes has significantly reduced the construction and purchase costs of force-feedback accelerometers, as discussed in section 2.4. While the micromachined accelerometers offer generally excellent performance, especially in terms of linearity, bandwidth and cost and power consumption, the manufacturers are still struggling to fix the serious problems of long-term stability.

Because manufacturers don't usually provide explicit specifications for aspects of their products exhibiting poor performance¹², it is vital that the accelerometers used in the CUSP System are thoroughly characterised. This verifies the manufacturer's specifications and exposes any undocumented characteristics that might affect the performance of the system.

The only low-cost accelerometer available in New Zealand in quantities applicable to the CUSP System is the Analog Devices ADXL105. Thus, the ADXL105 will be the accelerometer used for the CUSP System.

The ADXL105 is a surface micromachined silicon accelerometer. This results in very small sense mass ($0.5\text{mm} \times 0.4\text{mm} \times 2\mu\text{m}$, $0.5\mu\text{g}$ [65]) as it is produced by an etching and depositing process from a single wafer, rather than being produced by solely the etching of a physically large or composite wafer (i.e. the limitations of bulk micromachining) [66]. The sense mass is a beam and is suspended by springs attached to both ends, as shown in Figure 13 [67]. Small capacitive sensing elements are attached to the side of the beam mass and to the accelerometers body, as shown in detail in Figure 14 [68]. By a process of capacitive detection, the position of the 'finger' attached to the beam can be determined within the two surrounding, fixed, fingers.

¹² Often 'typical' specifications are given, with no guaranteed limits provided.

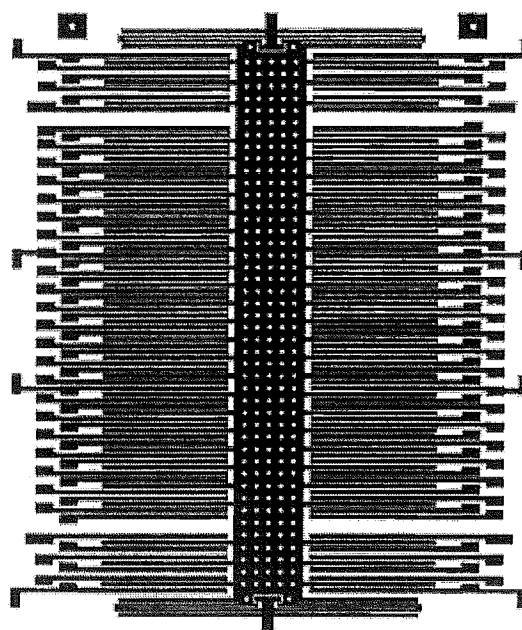


Figure 13, Beam and 'finger' sensing cells of ADXL105 accelerometer (from [67])

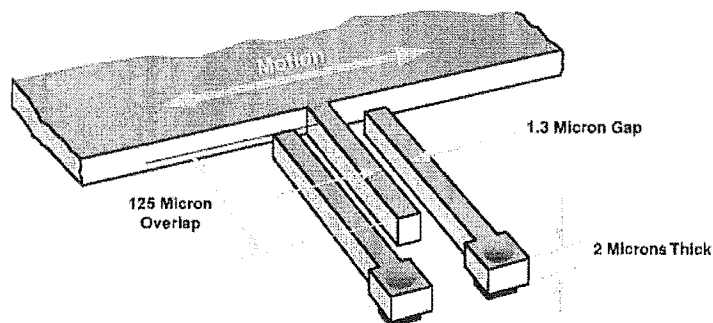


Figure 14, The 'finger' arrangement of the sensing cells of the Analog Devices MEMS accelerometers (from [68])

Analog Devices have found that better performance can be realised if the feedback loop that was present in their earlier product, the ADXL05, is removed [67]. Given the small deflection of the beam (1 nanometre per g [65]), the increase in accuracy of the capacitive deflection measurement system without the feedback loop was a worthwhile gain for a slight reduction in the bandwidth (i.e. reduced resonant frequency).

8.4.1 Characterisation of the ADXL105

The Analog Devices ADXL105 MEMS accelerometer integrated circuit (IC) is a “high performance, high accuracy and complete single-axis acceleration measurement system on a single monolithic IC” [40].

These sensor’s primary features are:

- 2 mg RMS resolution (sensor noise floor over 100Hz bandwidth)
- 0-10 kHz bandwidth
- Flat amplitude response ($\pm 1\%$) to 5 kHz
- Low power
- Ratiometric output versus supply
- User scalable output range
- On-die temperature sensor
- Additional operational amplifier
- Surface mount
- +2.7 V to +5.25 V single-supply

The noise floor specified means that the specification for the maximum resolution can be improved to 2mg RMS, as opposed to the design specification of 5mg RMS as defined in section 5.2.

The important tests when using the accelerometer in strong motion seismograph applications include:

- Noise output.
- Performance over temperature
 - Sensitivity.
 - Offset.
 - Step response to large changes in temperature.
- Axial alignment.
- Long-term stability.

These tests are described in more detail in the following section.

8.4.1.1 Noise output

The output noise is determined from a reference recording with a 16-bit data acquisition system over two bandwidths: 40 and 80 Hz. These two bandwidths represent the CUSP System's recording bandwidth and a reduced bandwidth option, which may prove to be a useful addition if improved noise response or lower data transmission rates are required. These recordings were made over a 10 second interval.

The noise levels recorded over the two bandwidths are shown in Table 15. Three accelerometers, aligned in orthogonal orientations, were tested to ensure that any significant deviations due to localised noise or orientation were highlighted. The sensors exhibit slightly better performance than specified by the manufacturer.

Table 15, Noise levels of three orthogonal accelerometers with no applied signal

0.1 – 40Hz bandwidth	RMS noise (mg)
X channel	1.2301
Y channel	1.1225
Z channel	1.2268

0.1 – 80Hz bandwidth	RMS noise (mg)
X channel	1.6151
Y channel	1.4946
Z channel	1.6476

The histogram plots of the samples recorded from these three sensors over an 80Hz bandwidth provides an idea of the type of noise present in the sensors output, these plots are shown in Figure 15. As can be seen from the histograms, even though the sample set is small, the output noise distribution is of a Gaussian form, indicating that the noise is indeed ‘white’ as stated by the manufacturer.

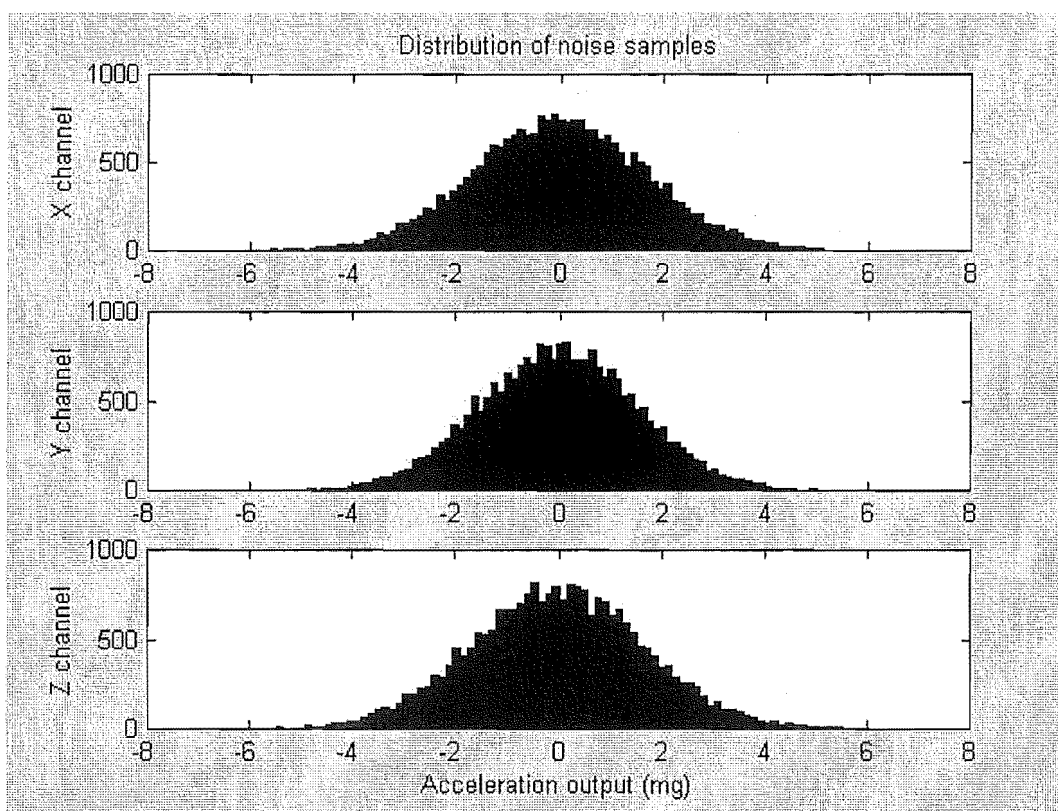


Figure 15, Histograms of the noise output of three accelerometer circuits, 0.1 – 80Hz bandwidth

To measure the low frequency noise, the device must be held at a constant temperature to avoid output changes due to slow thermal drifts. Several accelerometers were held at a constant room temperature and the output recorded over a 20-minute period, resulting in a frequency resolution of around 0.001Hz ($dF = F_s * 1.2 / N$, $F_s = 200\text{Hz}$, $N = 200\text{Hz} * 20\text{min} * 60\text{s}$). A typical spectrum of this test is shown in Figure 16, which clearly indicates that, while the noise spectrum is flat above 1Hz, below this frequency an undesirable $1/f$ relationship is apparent. It is not known whether this is due to slow temperature deviations below the resolution of the temperature measurements used, or due to electrical $1/f$ noise in the internal amplifiers and circuitry of the MEMS device. However, in either case, the inability to track this response by the temperature output makes this aspect a non-correctable characteristic.

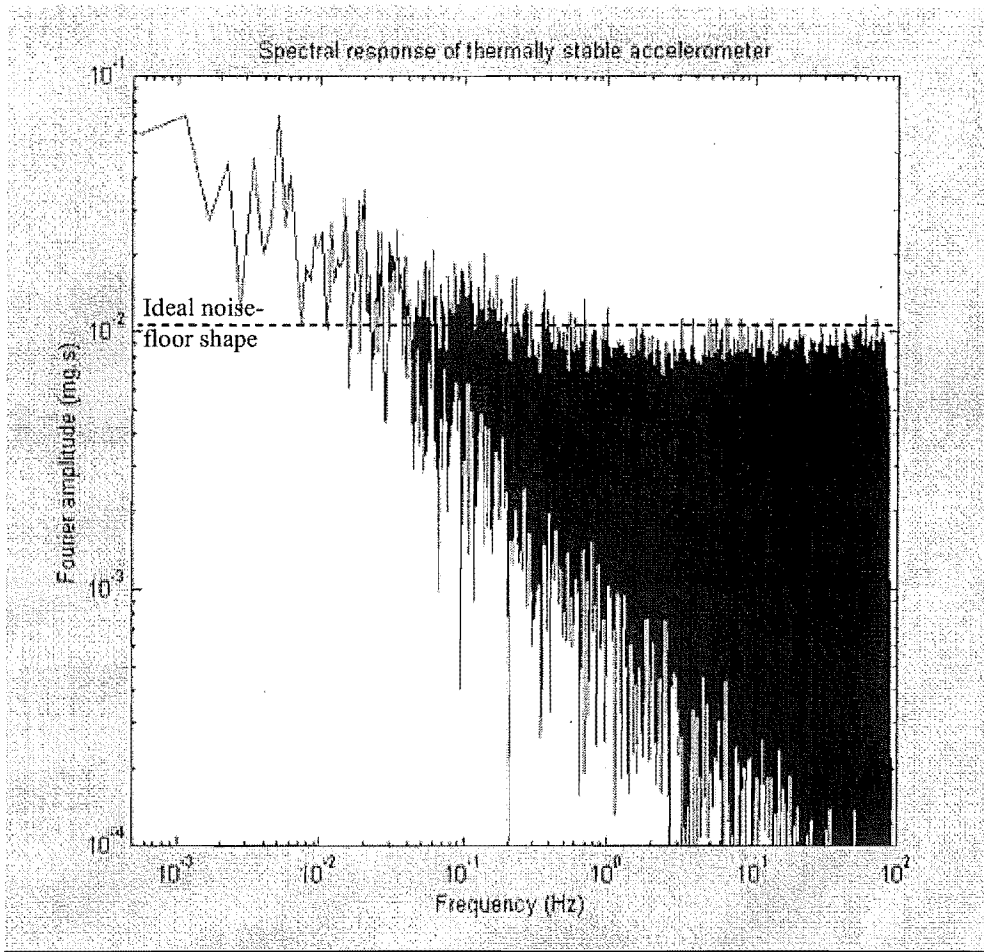


Figure 16, Noise spectral density of a thermally stable accelerometer, showing an undesirable increase in the noise floor at lower frequencies

8.4.1.2 Performance over temperature

An undesirable property of the low-cost micromachined accelerometers is their poor response to temperature fluctuations. The properties that respond to temperature changes include the offset and the gain of the transducer. This section aims to quantify these changes so that the scope of the problem is identified.

8.4.1.2.1 Accelerometers response to a temperature impulse

This test applies a temperature impulse directly to the body of the accelerometer, which measures any lag in the response time between the accelerometer's temperature and acceleration outputs. Ideally the temperature output will respond instantaneously

and proportionally to the acceleration deviation due to temperature. The temperature impulse was generated by directing a jet of hot air over a transducer, which was mounted on a printed circuit board. Because the relationship between the temperature and acceleration outputs is not expected to be linear, the test must measure the inflection points in the impulse response curves, and from these the delay between the temperature and acceleration outputs can be determined. The temperature and the accelerometer outputs are shown in Figure 17, where the scales have been matched to highlight any deviation.

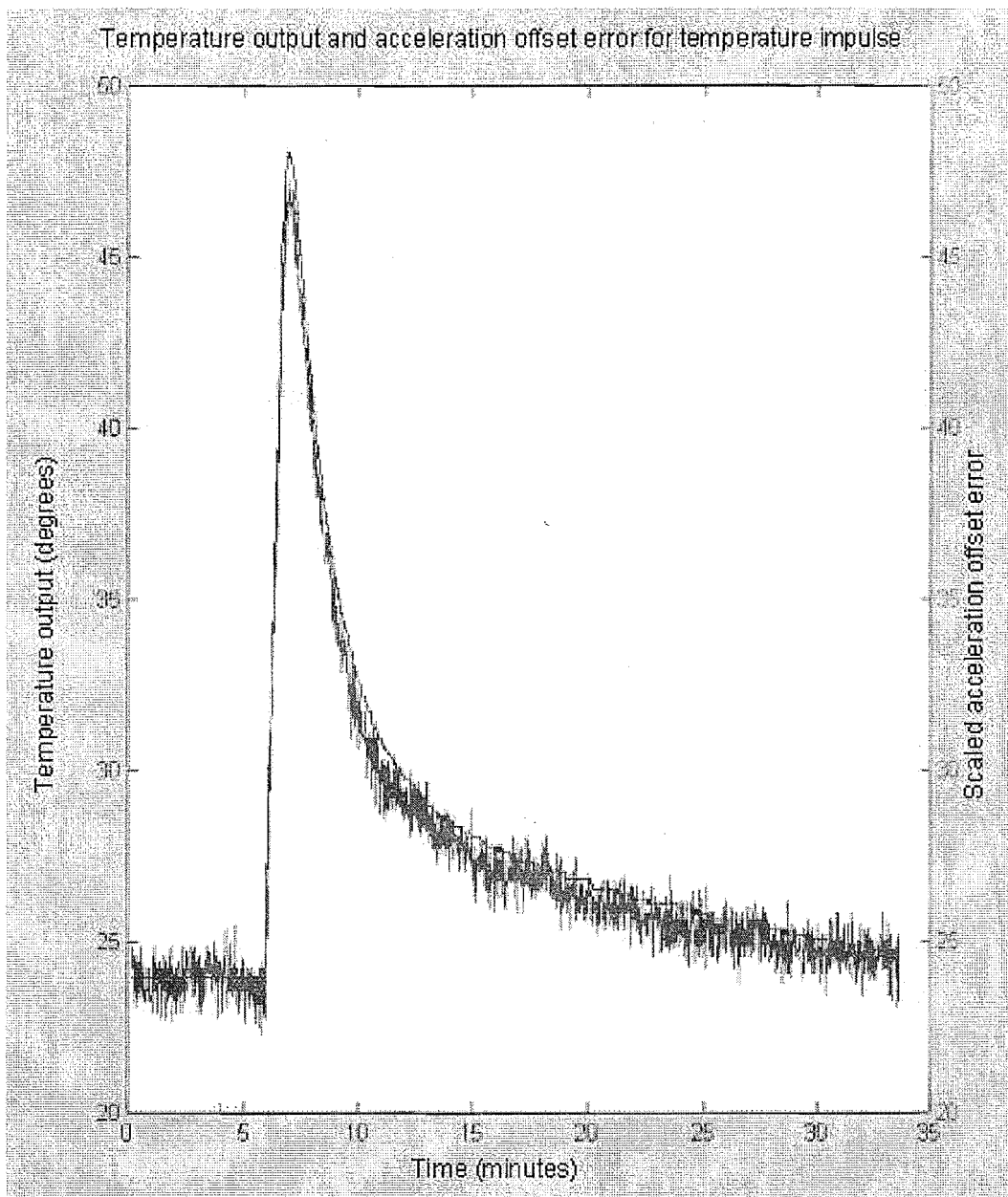


Figure 17, Direct heating of transducer, showing temperature sensor output and offset error

It is difficult to measure the precise delay value, because the accelerometer noise swamps any visible transitions, however, using a magnified view, no delay that exceeded five seconds was discernable.

8.4.1.2.2 Insulated temperature step response

This test applies a temperature step to the accelerometer via its housing when it is contained in a case similar to that anticipated for the final product. This determines the maximum temperature gradient that can be experienced by the accelerometer when protected by the thermal path of a typical enclosure as well as the thermal path between the accelerometer circuit and surrounding air and circuitry.

As Figure 17 shows, the response time between the acceleration output and the temperature sensor is essentially instantaneous. This permits the insulated response to be determined by the temperature output alone. The transducer was mounted on a circuit board inside a die-cast aluminium box, which was mounted inside a plastic enclosure containing a 10W dissipative element representing a processing platform. The entire system was then placed, unpowered, in a freezer. When the temperature stabilised, the power was applied and the system exposed to room temperature. This simulates the anticipated maximum temperature gradient expected in the real world; from unpowered operation at the minimum temperature of the instrument, to powered operation in morning sunlight. The results of this test are shown in Figure 18.

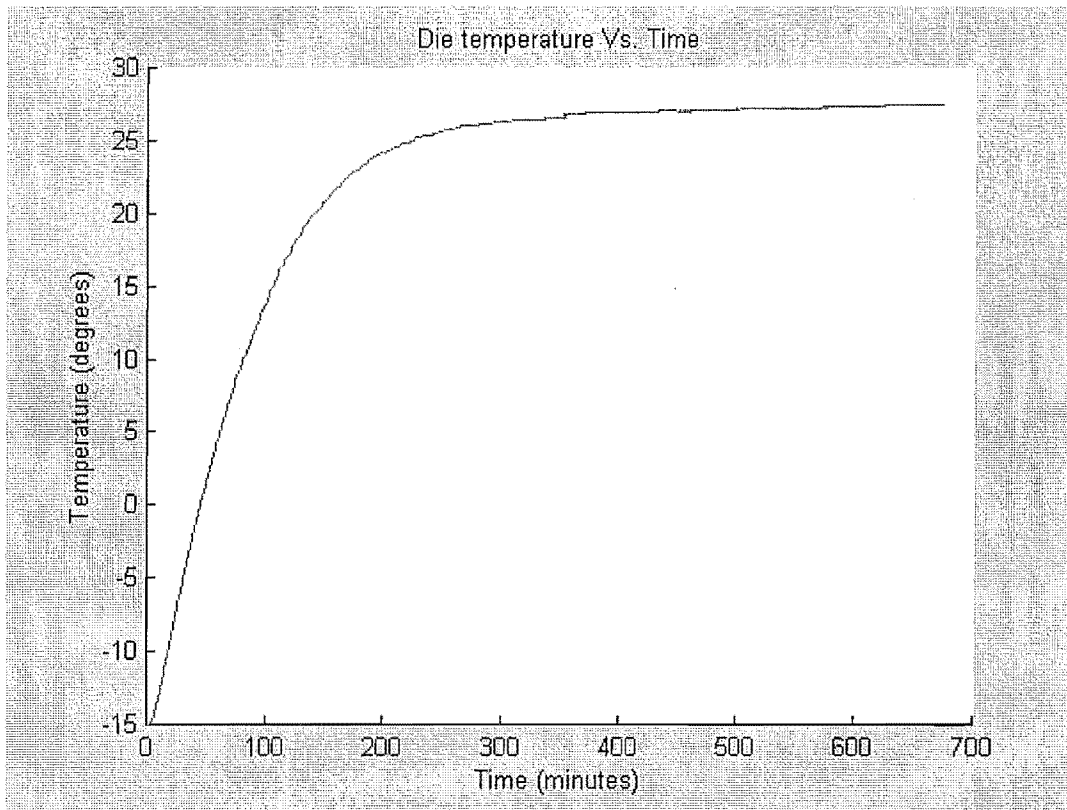


Figure 18, Temperature sensor output when subjected to the maximum anticipated temperature gradient

The steepest section of this curve gives a maximum temperature gradient of $6.45\text{m}^{\circ}\text{C}\cdot\text{s}^{-1}$.

8.4.1.2.3 Thermal offset error

One of the most widely discussed properties of silicon micromachined accelerometers is the offset change with temperature. This property is documented in the manufacturers datasheet and is given as $\pm 222\text{mg}$ over the entire temperature range [40].

What is not well documented (and not mentioned at all in the datasheet) is the hysteresis effect apparent on the output when cycled over temperature. Cycling 12 accelerometers over a temperature range of -5°C to $+55^{\circ}\text{C}$ while recording the offset at 16 discreet points on both the heating and cooling sides, resulted in the hysteresis loops shown in Figure 19.

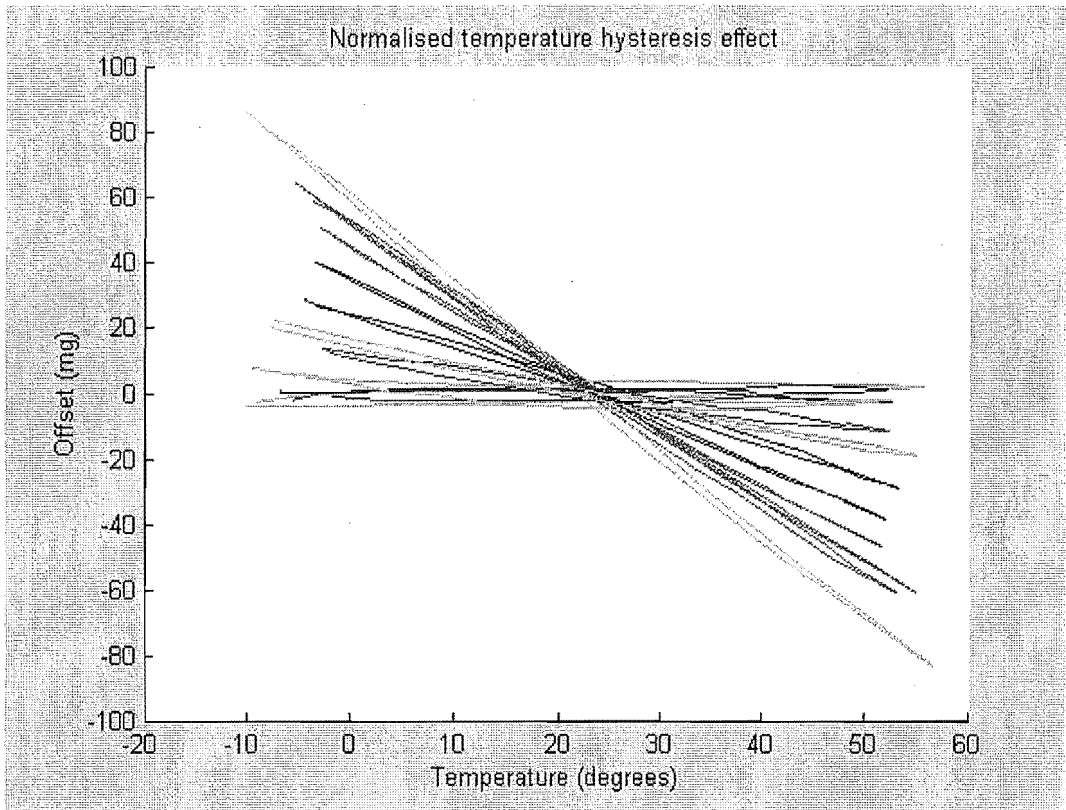


Figure 19, Hysteresis loops of 12 accelerometers offset points over temperature

The maximum hysteresis loop aperture in Figure 19 is 7mg. However, some devices recorded up to a 60mg offset when subjected to an thermal cycle from room temperature to -25°C and back.

Silicon Designs, another micromachined accelerometer manufacturer [69], recommends thermal cycling of their components once installed and orientated in the intended operation orientation. Their accelerometers also exhibit offset ‘sag’¹³ where the output droops when a constant acceleration is applied. This is also related to temperature, and the effect doubles every 35°C [70].

The use of micromachined technology for space applications, where large and abrupt changes of temperature occur, has prompted research that indicates a thermal ‘bimaterial’ effect occurs. This strains the device around points of contact between

¹³ Manufacturers name is ‘acceleration hysteresis’.

differing components of the micromachined device [71]. This would potentially explain the observed effects. The research suggests this problem improves with age as the device undergoes strain hardening; however no investigation has been performed on this aspect for the CUSP System. Unfortunately, discussion with a design engineer at Analog Devices micromachined products division suggests that cycling does not result in significant improvements to the hysteresis effects of their accelerometers [72].

By extrapolating the raw (i.e. non-normalised) centrelines of the hysteresis loops shown in Figure 19, the average offsets of 12 devices are shown in Figure 20. This figure clearly shows that the deviation due to temperature is swamped by the deviation due to the initial offset error. Although not clear due to the limited resolution of the figure, the actual offsets do not follow any fixed pattern (i.e. the error cannot be classified as any sort of low order polynomial curve) and in some extreme cases, kinks, or short regions of stepped offsets, are apparent in the offset error, only to return to the ‘trend’ after some small temperature increment.

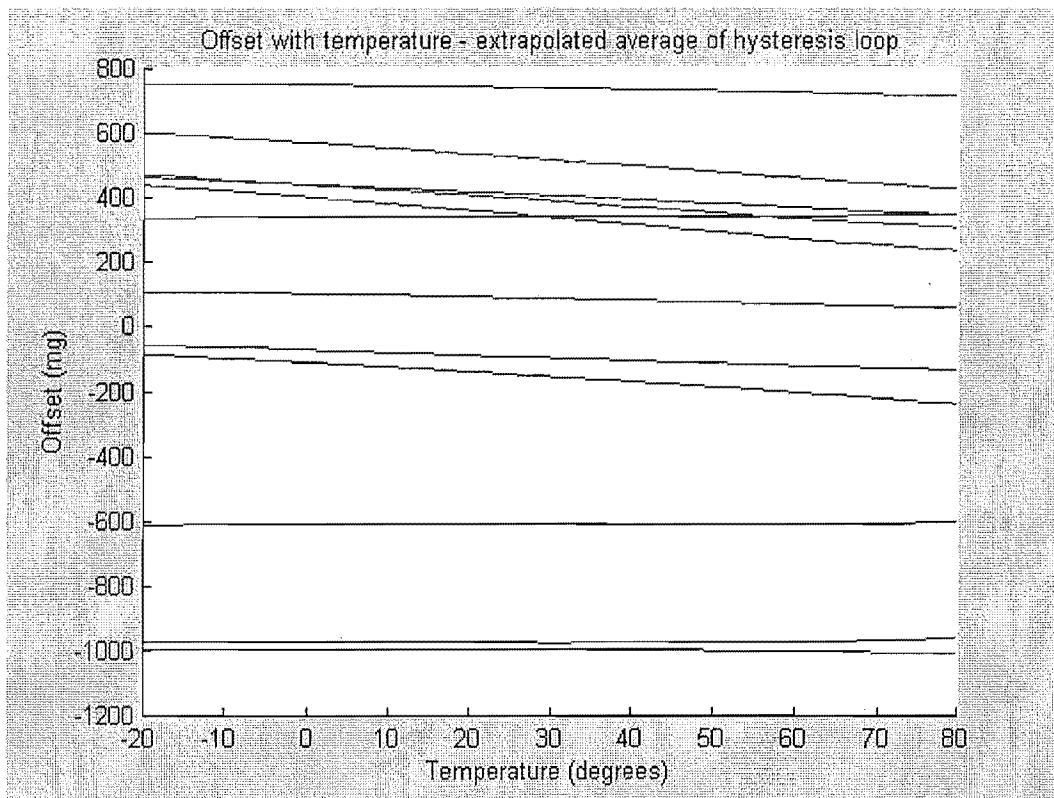


Figure 20, Extrapolated offsets resulting from averaging the offset hysteresis loops, indicating both the large effects of the offset, plus the variable response to temperature changes

8.4.1.2.4 Sensitivity

The sensitivity exhibits much more predictable properties than the offset error. No discernable hysteresis was observed and the sensitivity error appears to follow a straight line, with no exceptions found within the sample set. The sensitivity errors of 12 accelerometers are shown in Figure 21, with straight-line extrapolations to the devices temperature limits. The limits of this range lie slightly above the manufacturer's specified 'typical' error of $\pm 0.5\%$. However, since no maximum error is specified by the manufacturer [40], and the fact that the errors measured do not wildly vary, confidence is gained that the maximum error is unlikely to deviate too much from the typical value.

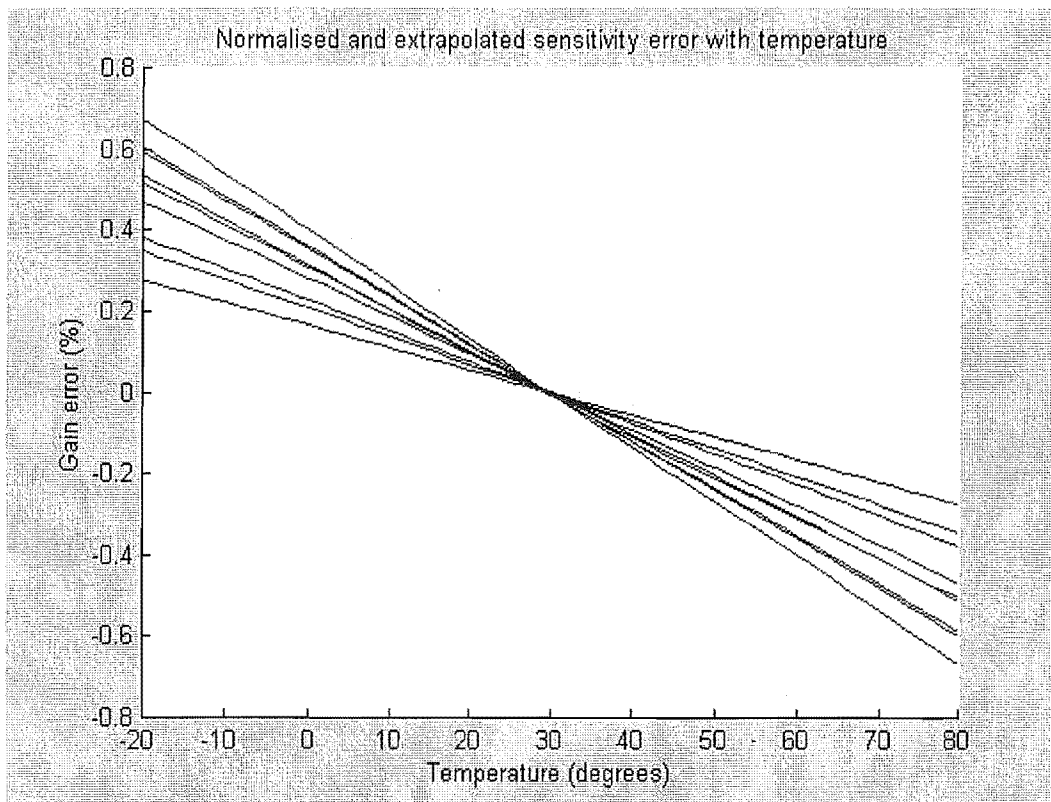


Figure 21, Extrapolated and normalised sensitivities for 12 accelerometers.

8.4.1.3 Axial alignment

The angular misalignment of the accelerometers must be ascertained to determine the quantity of cross-axis signals that are coupled into the signal. This test was performed with the devices wave-soldered onto circuit boards to provide a practical result that includes the angular misalignment resulting from the soldering process. This additional error should only be obvious in the horizontal alignment error. 39 accelerometers were subjected to a tilting routine that placed the sensitive axis perpendicular to the gravitational acceleration in both the horizontal and vertical planes of the sensitive axis, as shown in Figure 22, with the sensitive axes marked with the yellow arrow drawn on the accelerometer's body. Initially tests were performed over the operating temperature range but no discernable thermal effects were recorded. The remainder of the testing was performed at room temperature for simplicity.

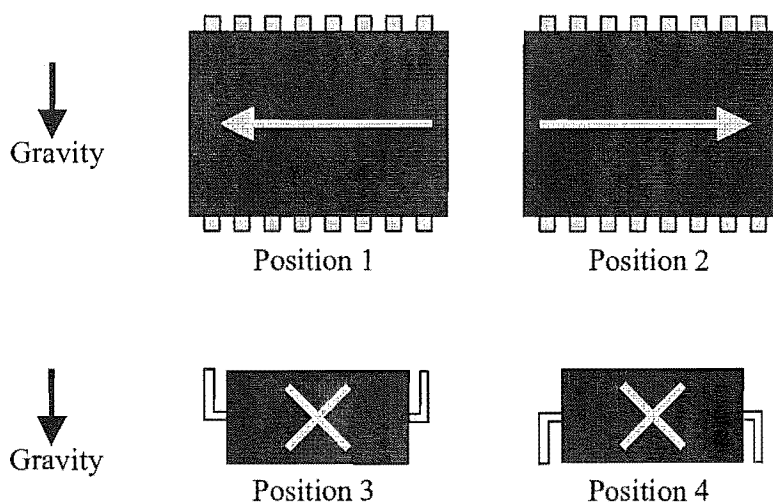


Figure 22, Orientations for determining the axis misalignment

The misalignment angles were calculated by trigonometric means from the ratios of the four output measurements to the value of the output with the sensitive axis aligned with the acceleration due to gravity. The resulting misalignment angles are presented as histograms in Figure 23 and Figure 24. These figures show the misalignment error in the horizontal plane and the plane of the sensitive axis and the direction normal to the mounting plane respectively.

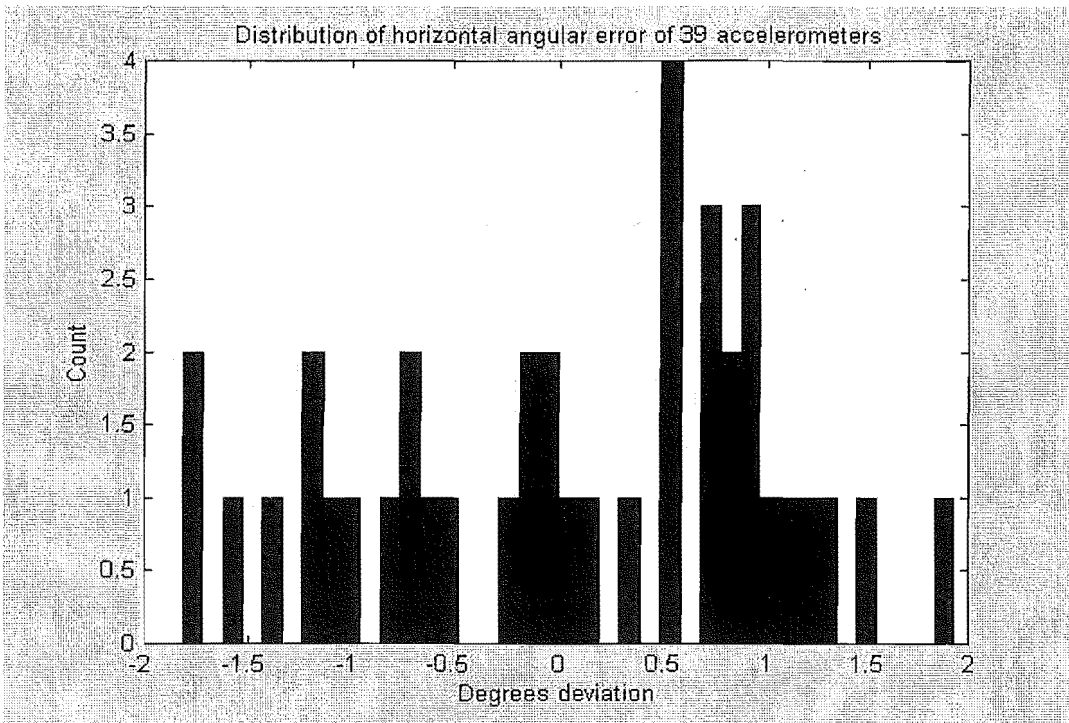


Figure 23, Degrees of axis misalignment in the mounting plane of the accelerometers

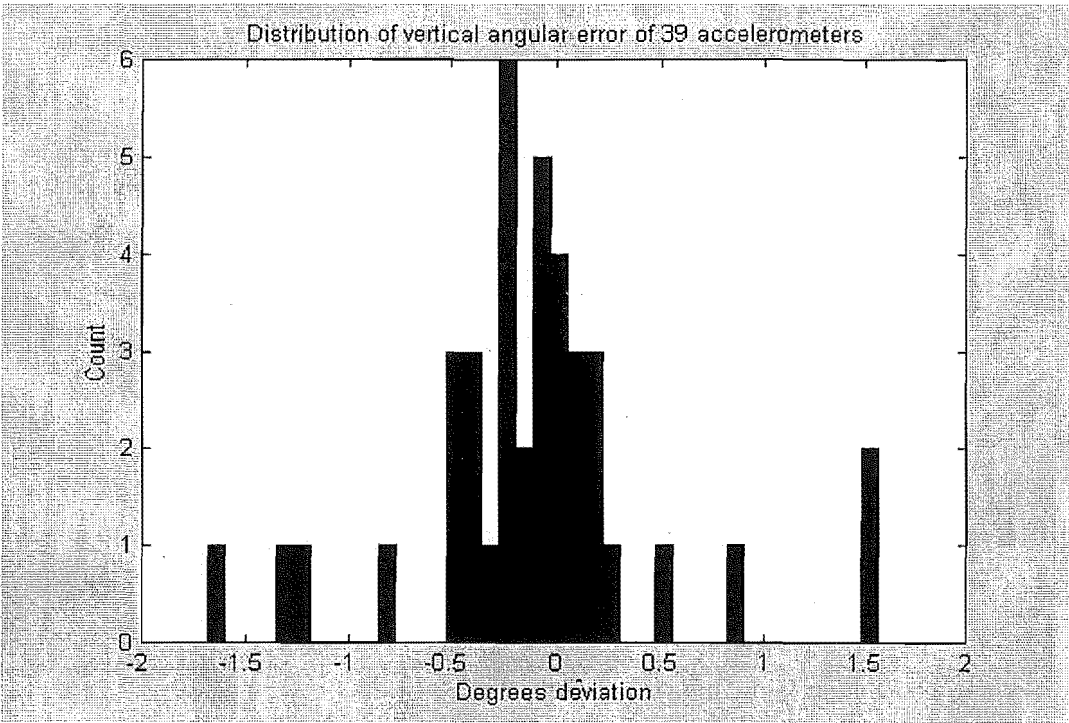


Figure 24, Degrees of axis misalignment in the plane normal to the mounting plane of the accelerometers

Figure 23 and Figure 24 shows a much more pronounced deviation in the horizontal axis, even though the span of the errors is similar. No tests were done to determine the component of the misalignment in the horizontal plane induced by the mounting process.

8.4.1.4 Long term stability

As no low-seismic-noise constant-temperature chamber has been available to the project, no quantitative measures can be given for long-term stability of the ADXL105 device. This results in the inability to predict long term accuracy of calibration or correction schemes.

8.4.2 Summary of the ADXL105 sensor

The characterisation of the ADXL105 micromachined accelerometer has indicated that the manufacturers datasheet is both optimistic with respect to ‘typical’ values and neglects to mention all the parameters affecting the performance of the devices. Discussions with the manufacturer indicates that their general device testing does not measure all the parameters specified to their limits [72], meaning that some devices may be released that are significantly worse than specified.

The temperature effects of the offset (neglecting hysteresis), as well as gain errors, can be easily corrected for by digital means via a lookup table that is indexed by the die-temperature. The axial misalignment can similarly be corrected digitally, in real-time, if the angles are measured and a correction matrix created.

The worst characteristic of the accelerometers is the effect of the temperature hysteresis on the offset. This error, whilst smaller than both the offset error due to temperature and the initial offset error, sets the absolute output error of the device, as it is not plausible to know the temperature history of the device necessary to provide correction. The error due to the hysteresis will therefore result in a zero-level window of up to $\pm 3.5\text{mg}$ when operated within the expected operating temperature range. However, testing with un-powered cooling to -25°C resulted in up to $\pm 30\text{mg}$ of offset.

If this error is not countered for, any triggering schemes using the absolute level will be compromised, as will any misalignment correction scheme. Furthermore, it will be impossible to distinguish between any offsets due to instrument tilting or hysteresis effects – $\pm 30\text{mg}$ offset equates to an angular deviation of $\sim 3.5^\circ$.

A further negative characteristic of the accelerometers is the presence of a non-correctable $1/f$ -type relationship in the low frequency noise spectrum, below about 1Hz. This results in negligible visible effects on the acceleration trace but will have serious consequences to the displacement records derived from double integration of the acceleration records. Even if this effect is occurring due to temperature fluctuations, because it was observed when the device was held at a constant temperature (i.e. below the resolution of the temperature measurement system) this aspect cannot be corrected.

A summary of these errors is presented in Table 16.

Table 16, Summary of ADXL105 characterisation

Initial offset range	$\pm 900 \text{ mg}$
Offset drift over temperature (-20 to +80°C)	$\pm 100 \text{ mg (worst case)}$ $\pm 2.5 \text{ mg } ^\circ\text{C}^{-1}$
Offset hysteresis effect with temperature cycling (-20 to +80°C)	$\pm 3.5 \text{ mg (typical)}$ $\pm 30 \text{ mg (worst case)}$
Gain change over temperature	$\pm 0.7\% \text{ (-20 to +80}^\circ\text{C)}$ $\pm 0.45\% \text{ (-10 to +50}^\circ\text{C)}$
Maximum rate of temperature change	$6.45 \text{ m}^\circ\text{C s}^{-1}$
Axial misalignment (PCB plain)	$\pm 2^\circ$

Axial misalignment (vertical plain)	$\pm 2^\circ$
Output noise	1.7 mg RMS (0.1 - 80Hz) (typical) 2.0 mg RMS (0.1 - 80Hz) (worst case) 1.2 mg RMS (0.1 - 50Hz) (typical) 1.5 mg RMS (0.1 - 50Hz) (worst case)

8.5 Calibration and correction of the ADXL105 sensor

8.5.1 Introduction

The characterisation process presented in the preceding sections indicates that there are several undesirable properties of the chosen accelerometers that must be corrected for. Furthermore, the output of the instrument must be consistent between units and referable to a common standard. The process through which this is achieved is calibration. The calibration process will be described after the correction process as the correction process contains steps that provide useful calibration data as a by-product.

8.5.2 Error corrections

The summary of the ADXL105 characteristics given in Table 16 shows that the worst aspect of these sensors is the temperature-induced hysteresis. This set a fundamental limit on the accuracy to which the zero level can be resolved, as the position on the hysteresis loop cannot be determined during operation of the instrument. The aim of the calibration and correction process must then be not to provide correction to an absolute zero point, but to provide a stable offset for the duration of a record. Thus, the pre-event data captured can be used to set the zero reference for the record.

While this approach result in the loss of information relating to the instruments tilt, it should be noted that the maximum hysteresis aperture size noted was $\pm 30\text{mg}$, which corresponds to a deviation of only $\pm 3.5^\circ$. Also, this shift cannot occur rapidly. For the full effect of a 60mg change to occur, the instrument has to have been exposed to $+80^\circ\text{C}$ in the past and must start at mid-span in the temperature ($+20^\circ\text{C}$), then to drop to -20°C , and raise again to $+20^\circ\text{C}$. For this cycle of $+20^\circ\text{C}$ to -20°C to $+20^\circ\text{C}$ to occur at a maximum temperature gradient of $6.45\text{m}^\circ\text{C s}^{-1}$, the time span must be in the vicinity of 10 days. Over the 60-second period of a typical record, less than $120\mu\text{g}$ of this offset change will occur, which is well below the instruments resolution. Therefore, because earthquake-induced tilt will occur as a result of an event, provided the instrument triggers, the tilt can be determined from the levels of the pre-event and post-event data.

To provide a stable baseline over the duration of the longest expected record, conservatively given as five minutes, the maximum allowable deviation due to temperature must be less than the instrument's resolution. With a maximum temperature gradient of $6.45\text{m}^\circ\text{C s}^{-1}$, and a maximum offset error of $\pm 2.5 \text{ mg } ^\circ\text{C}^{-1}$, the maximum error thus becomes $\pm 4.83 \text{ mg}$. This is clearly outside the instrument's resolution, indicating that some form of correction process for the offset is required.

The gain change over temperature of $\pm 0.45\%$ over the range of -10°C to 50°C is considered small enough to ignore full temperature calibration. Room temperature calibration will thus result in a maximum error of 4.5mg/g over the typical operating temperature range.

The axial misalignment of $\pm 2^\circ$ for both the mounting and vertical plains equates to some $\pm 3.5\%$ of cross-axis sensitivity. Although this is a worst-case specification as it includes placement alignment errors, and although the effect is smaller than the sensitivity error that is ignored, some form of correction is required for this aspect as it correlates the channels.

Therefore, the corrections required for the ADXL105 MEMs accelerometer are thus:

- Correction of temperature induced offset drift
- Correction of the axial misalignment

The methods to provide these corrections will be discussed in the following sections.

8.5.2.1 Temperature induced offset correction

As discussed in section 7.2.4, digital correction methods are the preferred approach to removing any temperature induced offset errors. This is due to the repeatability and stability, the ease of adjustment, and the lack of signal distortion effects offered by digital systems.

The most obvious, and simplest, method for correcting the offsets is to subtract the known offset for a given temperature, determined by data stored in a look-up table of predetermined errors. This implies the knowledge of the temperature of the accelerometer being corrected. Fortunately this ADXL105 has an analogue temperature output that can be easily measured with the internal A/D converter available on most low-cost microprocessors. Thus, the correction process requires a table of offsets for a given accelerometer and access to the accelerometer's die temperature.

As discussed in section 8.4.1.2.3, the offset error is not simply a single line of temperature-stimulated offsets. The hysteresis effects result in an uncertainty of the exact offset, which depends on the thermal history of the device. In order to minimise the error, the measurement of the offset errors must encompass the maximum and minimum in-use temperatures of the device and use the midline of the hysteresis loop.

The maximum thermally induced offset swing of $\pm 100\text{mg}$ must be corrected to within ± 0.5 least significant bits (LSB) of the acceleration A/D conversion to remain undetectable. Thus the $\pm 100\text{mg}$ range must contain $2 \times \pm 100\text{mg} / \pm 3\text{g} \times 2^{\text{RESOLUTION}}$ steps. As the acceleration conversion requires a minimum of 13 bits with the ADXL105's (Avery [73], section 4.3.3.2.1), the temperature correction must contain a

look-up table indexed by 10 bits of temperature data. This results in a correction table consisting of 1024 points, each containing a 13-bit offset correction value. For the three accelerometers, this equates to over 6kB of data if two 8-bit bytes are required for each 10-bit correction point. This is clearly too large a table to be stored inside a low-cost microprocessors re-programmable non-volatile memory.

The solution to this problem is to create a table with a 7-bit index, and interpolate the remaining 3 bits (8 points). This reduces the look-up table size to less than 1kB, a much more realisable proposition.

8.5.2.2 Axial misalignment correction

Because the misalignment occurs in both planes containing the sensitive axis, the output of the three orthogonal sensors will be correlated. In other words, all the sensors will, to differing degrees, respond to an acceleration applied solely in the direction of just one of the sensors. The method to correct for the cross-axis effects must perform the correction on all three channels simultaneously. The simplest way to do this is by the use of matrices.

The matrix shown in equation 11 describes the measured acceleration, distorted by the misalignment matrix. The 'A' terms denote the actual applied acceleration, in the direction described by the subscripted term. The 'M' terms denote the acceleration measured by the transducers described by the subscript. The 'X', 'Y' and 'Z' terms denote the three accelerometers outputs when aligned in the direction denoted in the subscript. For example, X_X denote the output of the X channel accelerometer with the applied acceleration in the X direction, Z_Y denotes the Z channel accelerometers output, with an acceleration applied normal to the sensitive axis in the Z-Y plane.

$$\begin{bmatrix} M_X \\ M_Y \\ M_Z \end{bmatrix} = \begin{bmatrix} X_X & X_Y & X_Z \\ Y_X & Y_Y & Y_Z \\ Z_X & Z_Y & Z_Z \end{bmatrix} \begin{bmatrix} A_X \\ A_Y \\ A_Z \end{bmatrix} \quad 11$$

Determining the magnitudes of the components of the misalignment matrix involves orienting the orthogonal transducers in all possible orthogonal orientations as depicted in Figure 25, and using the earth's acceleration due to gravity as the stimulating acceleration.

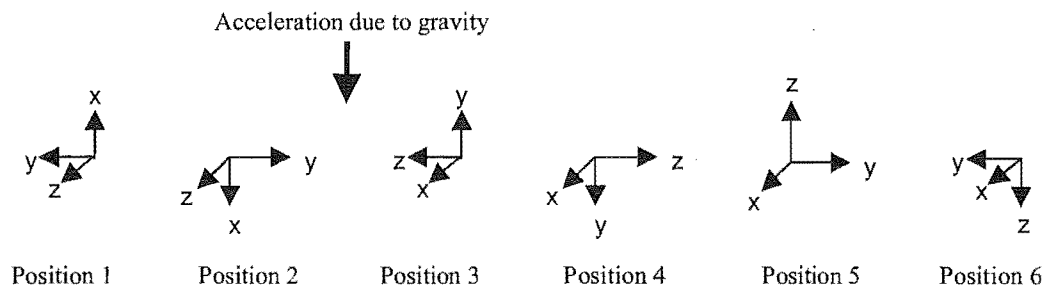


Figure 25, Transducer orientations used to determine axial misalignment.

The results of the data gathered by the scheme represented by Figure 25 provide six measurements for each accelerometer, three of which are of the opposite magnitude, which allows the determination of the true magnitude by subtraction of the magnitudes and division by 2. This process is described by equations 12, where the numbered subscripts denote the position in which the measurement was recorded.

$$\begin{aligned}
X_X &= \frac{X_1 - X_2}{2} \\
X_Y &= \frac{X_3 - X_4}{2} \\
X_Z &= \frac{X_5 - X_6}{2} \\
Y_X &= \frac{Y_1 - Y_2}{2} \\
Y_Y &= \frac{Y_3 - Y_4}{2} \\
Y_Z &= \frac{Y_5 - Y_6}{2} \\
Z_X &= \frac{Z_1 - Z_2}{2} \\
Z_Y &= \frac{Z_3 - Z_4}{2} \\
Z_Z &= \frac{Z_5 - Z_6}{2}
\end{aligned}
\tag{12}$$

Once the misalignment matrix is determined, the correction matrix is simply the inverse of this matrix, as shown in equation 13.

$$\begin{bmatrix} A_X \\ A_Y \\ A_Z \end{bmatrix} = \begin{bmatrix} X_X & X_Y & X_Z \\ Y_X & Y_Y & Y_Z \\ Z_X & Z_Y & Z_Z \end{bmatrix}^{-1} \begin{bmatrix} M_X \\ M_Y \\ M_Z \end{bmatrix}
\tag{13}$$

Because this matrix will contain some values near zero for small deviations, and the mathematical operations required to implement the matrix are multiplications, the precision to which this correction must be applied is difficult to achieve in an integer processor. Therefore, because the axial misalignment error is not changing with temperature and because the data acquisition subsystem will perform some of the data processing in the central processor subsystem, it is desirable to perform this correction process in the central processor subsystem as well. This necessitates the storage of the correction matrix in the data acquisition subsystem to maintain the self-containment requirement, and therefore transferral to the central processor subsystem before data acquisition begins.

8.5.3 Calibration and correction

8.5.3.1 Determining the temperature induced offset

In principle, the method to determine the temperature induced offsets is to apply a temperature sweep to the accelerometers and to record the acceleration and temperature outputs. Unfortunately, this process is complicated by the fact that the devices exhibit a hysteresis effect. The result must then be a compromise, as it is impossible to determine on where in the hysteresis loop the instrument will be operating. The calibration process thus performs two sweeps, one with increasing temperature and the other with decreasing temperature. These two sweeps will be averaged and the resulting calibration data the best compromise.

Because the temperature takes a long time to stabilise due to the insulating effect of the calibration equipment, the calibration process must be completed stepwise. This ensures that there is no lag between the applied temperature stimulus and the accelerometers output. Stability is tested by measuring the acceleration and temperature outputs over a time interval, and waiting until the slope of the data measured over this interval reduces below a threshold. The number of steps was experimentally determined to be 15 on each the cooling and heating cycles, which represents the best compromise between the calibration time and accuracy. Each data point is averaged over some thousands of samples to ensure that the recorded data

point represents the true average value. Though the number of samples averaged is somewhat higher than required, it is retained as it is available as part of the stability test routine.

8.5.3.2 Determining the axial misalignment

The method utilised to collect the axial misalignment data is simply to measure the output of the accelerometers in the six orientations shown in Figure 26. However, as the same issue of temperature stabilisation times apply to all measurements made, the same stability tests and averaging routines used in the offset error measurement are used to measure the accelerometers outputs.

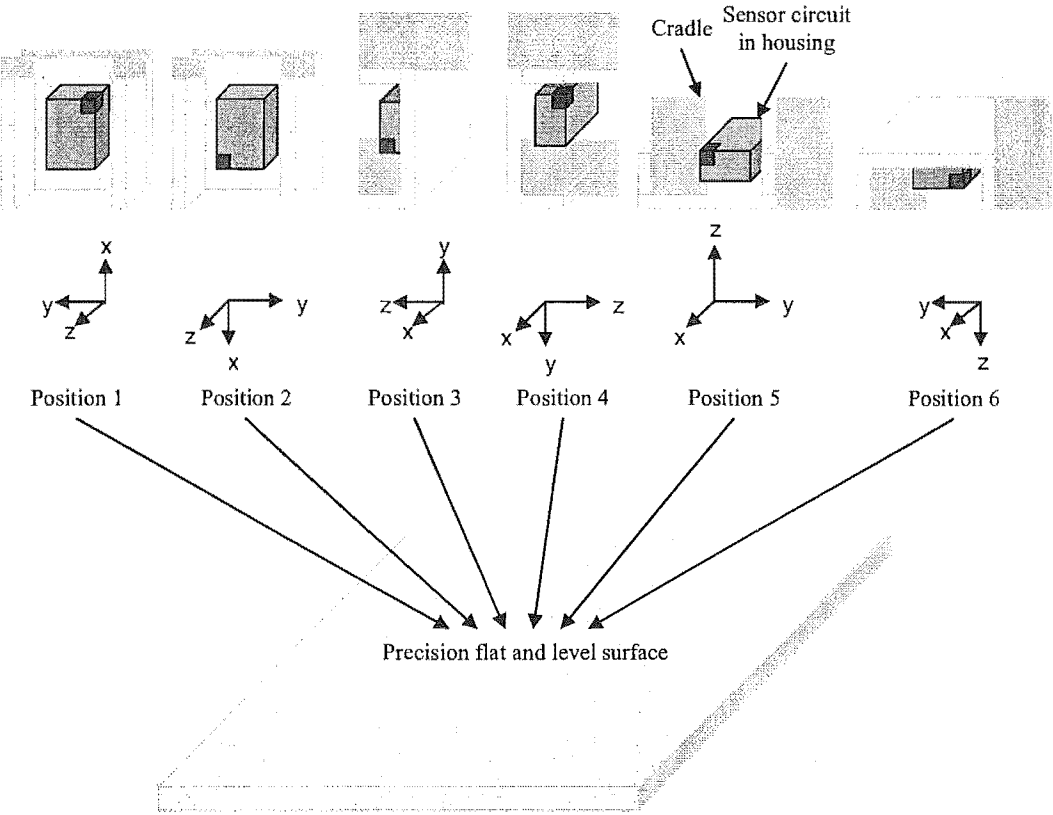


Figure 26, Transducer orientations used to determine axial misalignment (and gain).

Once the six measurements are made, the correction matrix can be determined mathematically.

8.5.3.3 Determining the gain adjustment values

Because the calibration of the axial misalignment contains the gain information at room temperature as part of the raw correction matrix, by neglecting to normalise the matrix, the gain correction is thus included in the correction process for the axial misalignment.

8.5.3.4 Calibration equipment

The equipment utilised to collect the temperature induced offset and misalignment data is shown in Figure 27 and Figure 28. The heating and cooling effects are provided by a Peltier-effect semiconductor heat pump attached to the transducer housing, which is wrapped in thermal insulation. The Peltier device is powered by a pulse-width modulated (PWM) power supply, which is, in turn, controlled by a PC application that also reads the acceleration and temperature outputs. A large thermal mass consisting of around 80 litres of water is used as a thermal reference point for the Peltier device.

The transducers are mounted in a frame that can be oriented in any orthogonal position, which is used for determining the misalignment and gain settings, and this frame lies on a precision flat and level surface. Thus six orientations with respect to the acceleration due to gravity are possible.

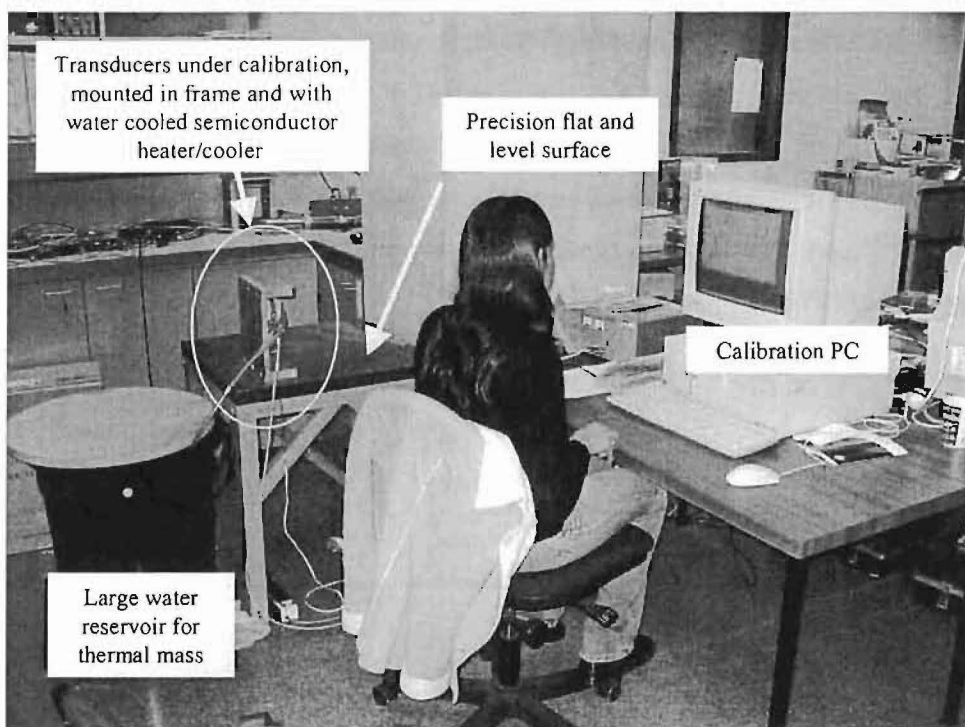


Figure 27, Overview of calibration equipment

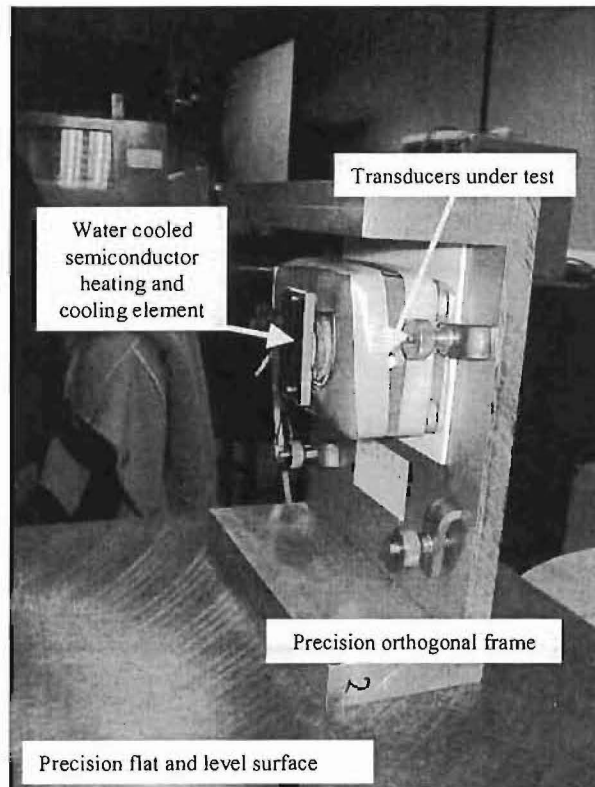


Figure 28, Close-up of transducer calibration frame, distortion is apparent due to lens effects

The application used to control the PWM power supply, and thus the temperature, reads the raw acceleration and temperature readings from the data acquisition subsystem under calibration. Once the data has been acquired, the application performs the processing discussed in the following section. The main page of this is shown in Figure 29. This application was developed by the author, in conjunction with Mr Peter Coursey.

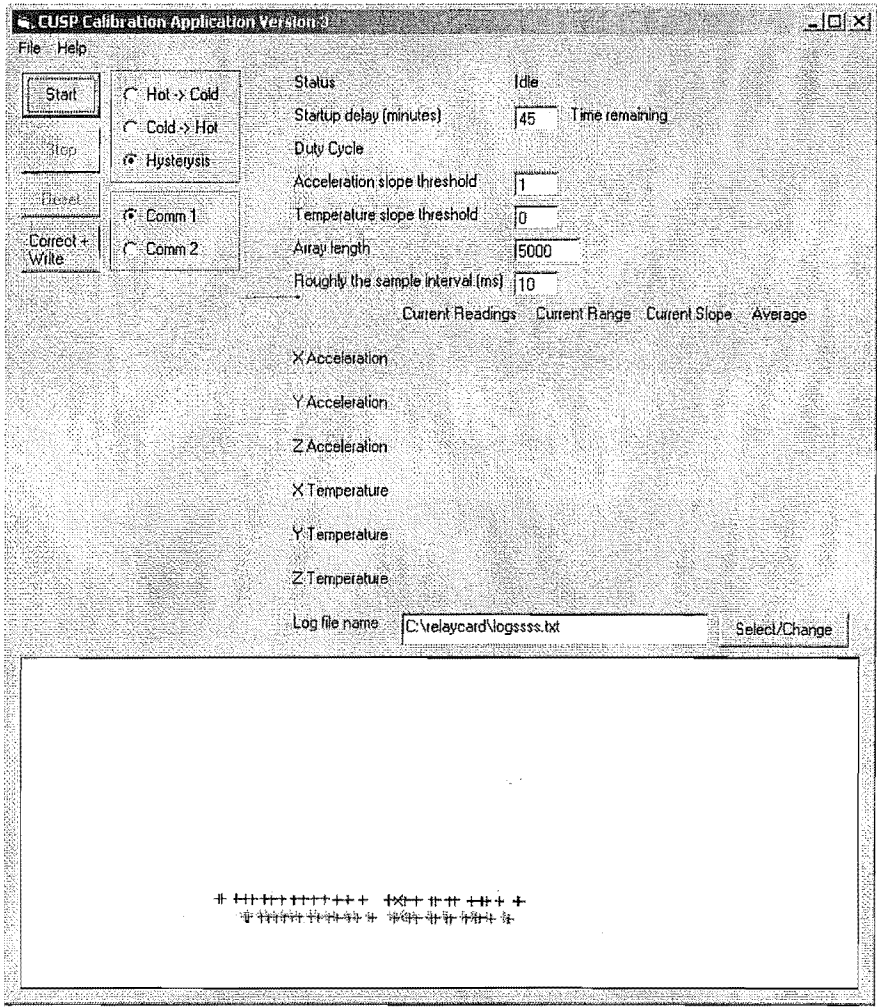


Figure 29, Calibration temperature sweep controller and data acquisition application

8.5.3.5 Calibration and correction data set processing

Once the offset data is acquired, the acceleration and temperature samples at the 15 discrete temperature points of the heating and cooling sweeps are interpolated to provide both heating and cooling curves. This means that if the 15 temperatures used for each side of the loop are not taken at exactly the same temperatures, the result of the averaging process is still valid. Once the two curves are created, the centreline of the loop is determined and the resulting curve extrapolated linearly to all temperature points outside the loop. This process can be seen in Figure 30, which shows the hysteresis loop from the 15 heating and cooling points and the interpolated centreline.

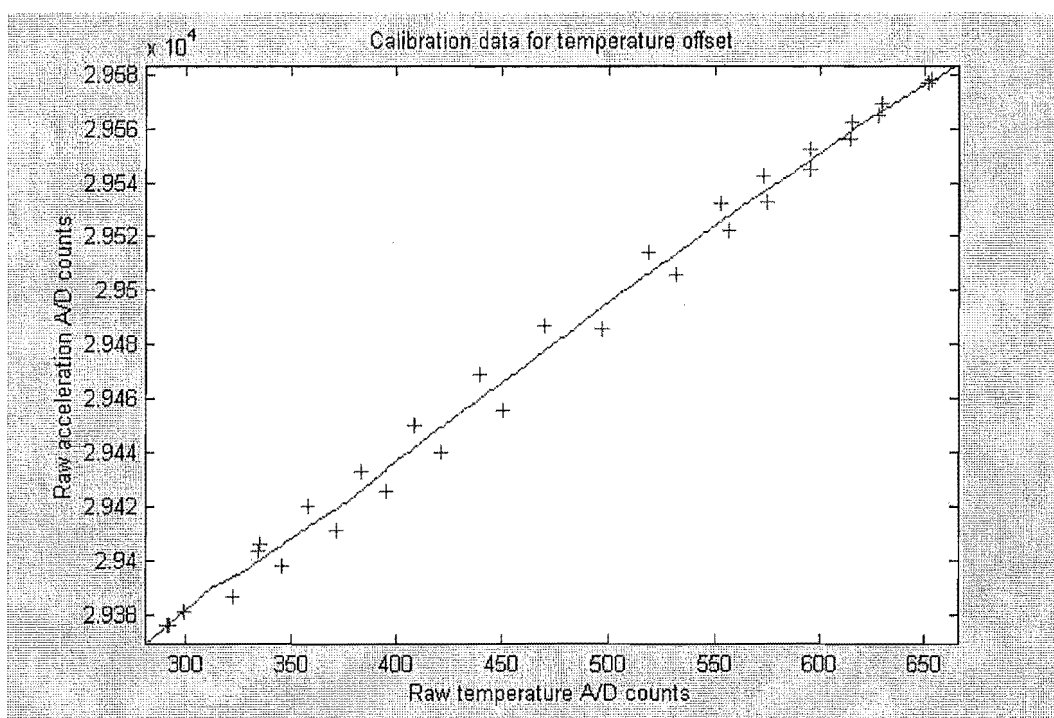


Figure 30, Hysteresis loop of temperature offset, showing interpolated centreline

Once the curve of the temperature-induced offset error is processed, the 1024 temperature points are decimated to 128 points, reducing the number of correction table points requiring storage in the microprocessor of the data acquisition subsystem, as discussed in section 8.5.2.1.

The axial misalignment and gain correction matrix is converted into an integer representation by multiplication and truncation. This allows a high precision number

to be stored in a large integer constant. These can be downloaded from the data acquisition subsystem before signal processing begins, and the converted back into the original floating point representation.

8.6 Results

While the correction and calibration process has proven possible, due to the long time needed to stabilise the devices after a temperatures change, the process take some 8-12 hours to cycle through. This means only one or two devices can be calibrated per day, which, for commercial production, would seriously reduce, or even eliminate, and price advantages of the low-cost MEMS devices. This problem must be addressed by future work.

Testing of the effectiveness of the process will be presented in the testing section of chapter 9.

8.7 Conclusions

The characterisation of the ADXL105 MEMS accelerometers indicates that, while most of the errors inherent in these devices can be corrected, the unspecified temperature hysteresis makes it impossible for these sensors to be used for long-term measurements, unless the temperature is stabilised. This is not considered to be of concern for the intended strong motion applications due to the short event record durations and the access to pre-event data, which provides an initial offset for the record.

The low frequency noise discovered also presents undesirable and non-correctable characteristics. While the magnitude of this error is significantly lower than that of the hysteresis problem, the small deviations, even over a short strong-motion type record, will result in significant deviations in the displacement records derived by double integration of the acceleration.

In general, the significant price advantage of the ADXL105 sensors outweighs the low performance, and the calibration and correction scheme presented in this chapter largely results in an acceptable performance level.

9 Subsystem design, construction and testing

9.1 *Introduction*

Chapter 7 outlined the requirements of the subsystems that constitute the CUSP System, and basic implementation issues were discussed at a general level. In this chapter, the design and construction of the instruments subsystems are discussed in more detail, and the general approaches that are adopted are presented. The detailed design work itself is described by Avery [73].

Following the discussion of the implementation, the final design specifications are presented. The final stage of the design cycle, testing, is presented last, as a validation of the design and verification of the specifications.

9.2 *Design and construction of the subsystems*

9.2.1 *Introduction*

This section aims to summarise the main design issues encountered in the implementation of each of the subsystems defined in chapter 7 and how these issues were resolved.

9.2.2 *Central processor subsystem*

Section 3 of Avery [73] describes the design process for the central processor subsystem. The section begins with choosing the type of processor to be used for the CUSP System. While the high-level decision is to use an x86 processor platform, the level of performance required has to be ascertained (bus width, clock rate, floating point support etc.), as well as which additional features (such as expansion bus protocols, storage media ports etc.) are required and the quantity of random access

memory (RAM) to be provided. These parameters affect the overall power consumption, form factor and performance, as well as cost. Since the Linux operating system is to be used, and because Linux operates on all the x86 platforms, a desktop PC was used for the initial development. Once the final requirements were determined, a platform was chosen that meets the minimum performance level, thus preventing excessive power consumption.

9.2.3 Data acquisition subsystem

The design of the data acquisition subsystem begins with a summary of the specifications and design approaches for the system that are given in the earlier chapters of this thesis. From these requirements, a number of sub-components to the data acquisition system are identified, namely: the transducers, the sampling system, a command, correction and control microprocessor, a power supply and the interface to the central processing subsystem. A design map of these components is created, as shown in Figure 31, and approaches taken to implement them are discussed individually.

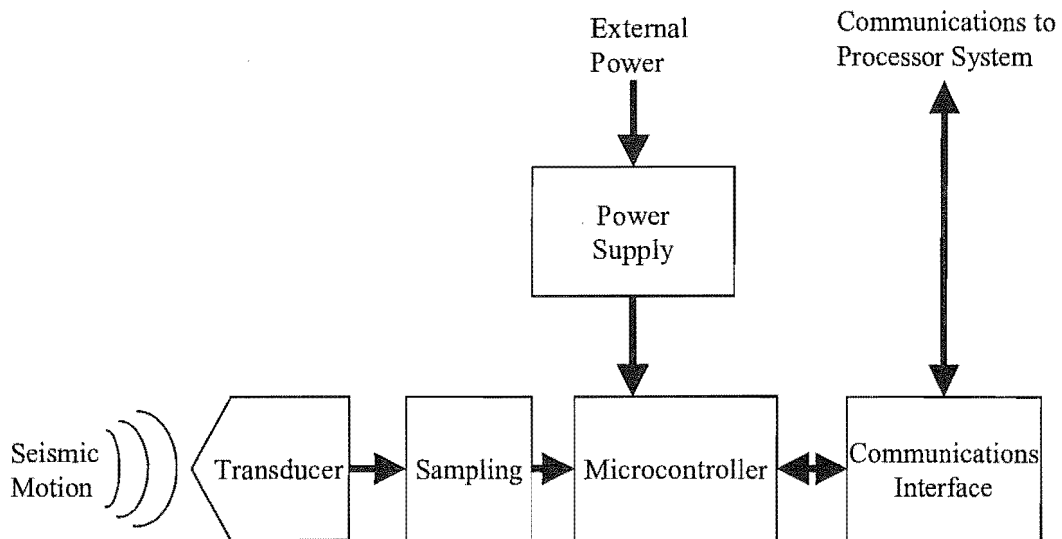


Figure 31, Data acquisition subsystem block design

The sub-component design process is presented next. This begins with a generalised discussion on the component choices and availability. The detailed design process for each sub-component includes the identification the best choice for the components to realise the required functionality and performance, a discussion on how the chosen components will interact, and the development of a working circuit. The resulting circuits are then collated into a final circuit, and a diagram of the data flow through the completed system is presented. Construction issues relating to the development of

a low-noise device for seismic monitoring purposes are discussed and the printed circuit board is presented, as shown in Figure 32.

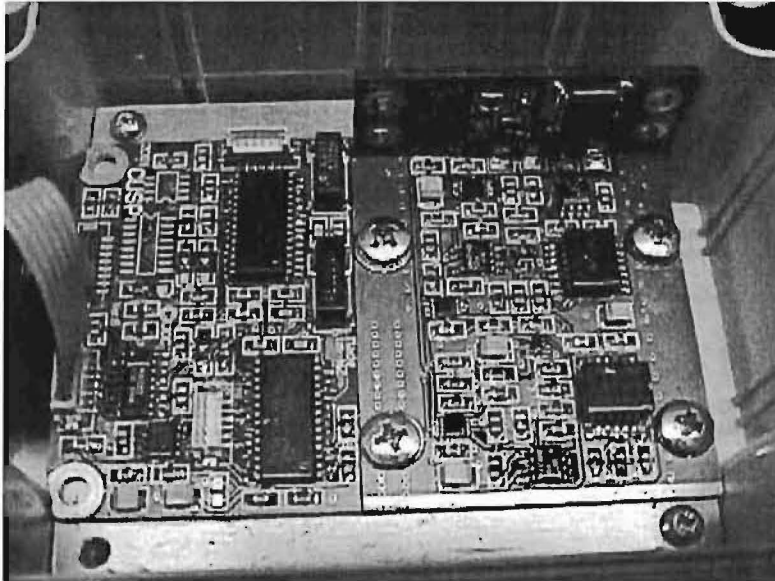


Figure 32, Complete data acquisition subsystem hardware

Because the data acquisition subsystem contains a microprocessor for correction of the errors in the response of the chosen MEMS sensors, as well as general command and control of the subsystem, a discussion on the development of the software is included. Section 4.6 of [73] describes this software design process and begins with an outline of the tasks required of the microprocessors. A graphical representation of the data flow through the subsystem is developed to aid the understanding of the interactions between the hardware and the software, and is shown in Figure 33. From the written requirements and the graphical data-flow diagram, the software tasks are divided into modular routines. This aims to increase code testability and maintainability as well as to help simplify the understanding of the process. Each of these routines is discussed in detail and the module flow charts are presented.

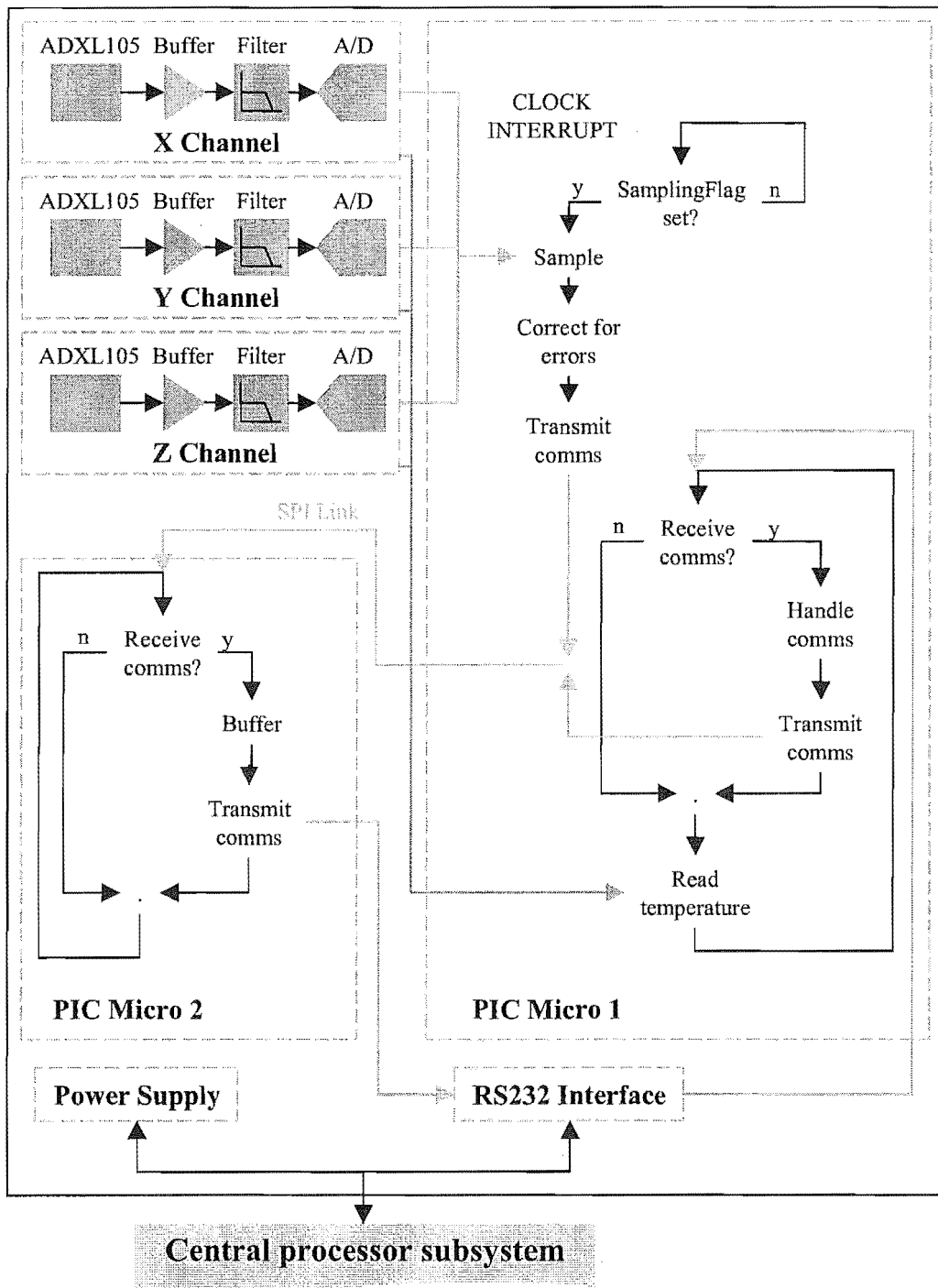


Figure 33, Data acquisition subsystem data flow and software functionality

9.2.4 Time signal generation subsystem

Design of the time signal generation subsystem begins by presenting a summary of the requirements for this subsystem, and then determines the detailed approach to realise these requirements. A graphical representation of the subsystem is presented, as shown in Figure 34, which indicates that the subsystem can be broken into four hardware sub-components, a COTS GPS receiver, a communications interface, signal level conversion circuits and a power supply.

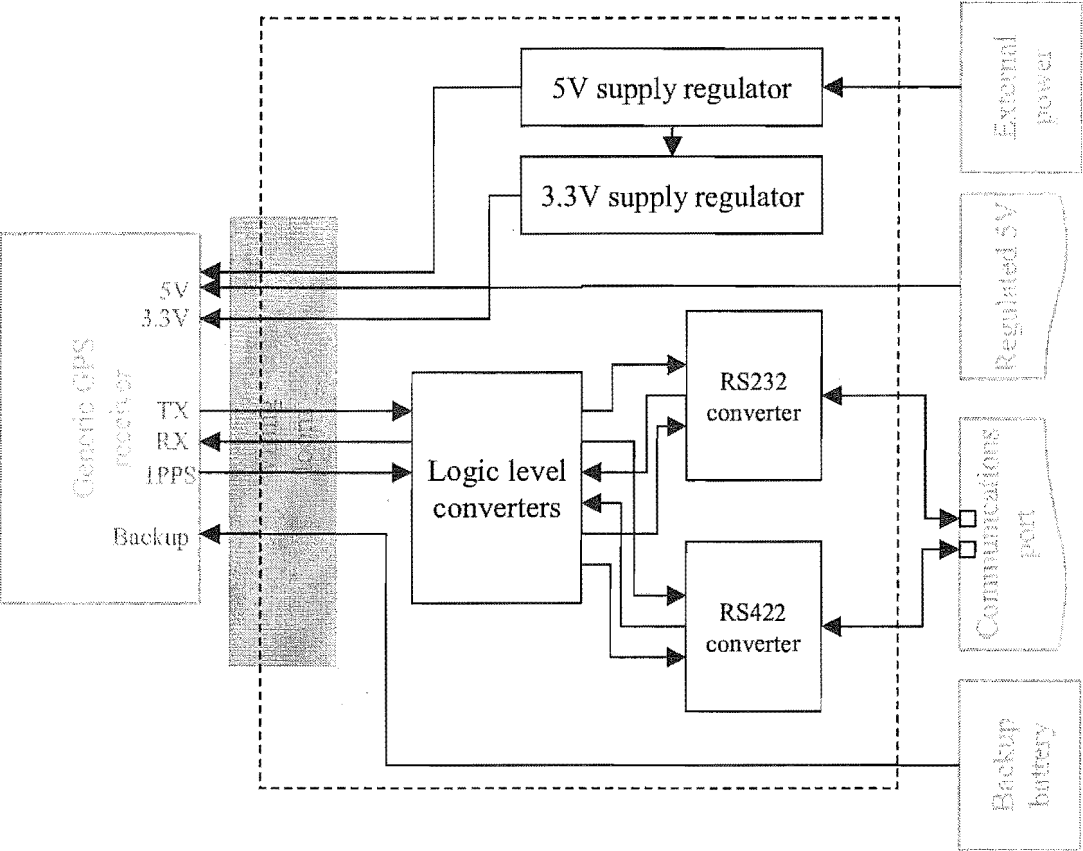


Figure 34, Block design of time signal generation subsystem hardware

As the GPS receiver is to be a COTS device, the designs of the remaining three sub-components are the presented and a final circuit developed. Issues relating to the construction of the physical circuit are discussed and a printed circuit board presented.

9.2.5 Communications hardware subsystem

As the communications hardware is to be entirely COTS manufacturer supplied, no discussion of this component is presented.

9.2.6 Power supply subsystem

The design of the power supply subsystem, presented in section 7 of [73], begins by reviewing the power supply's requirements defined in the previous chapters of this thesis. A summation of the power demands of the designs for the other subsystems is made. A detailed design specification is then developed by the collation of the required tasks and the summed power requirements.

The design is then broken into obviously similar tasks, these being; the interface to the central processor subsystem, the power regulators, the protection circuits, the health monitoring circuits, controlled outputs for devices like modems and the data acquisition subsystem, and some overall control circuitry including a user control switch. The operation of the system is then defined in a flow chart that indicates the desired logical sequences and delays required, to, for example, allow Linux to shutdown before the power is switched off. A graphical representation of the power supply subsystem is then presented that indicates the signal paths as well as the power paths, and is shown in Figure 35.

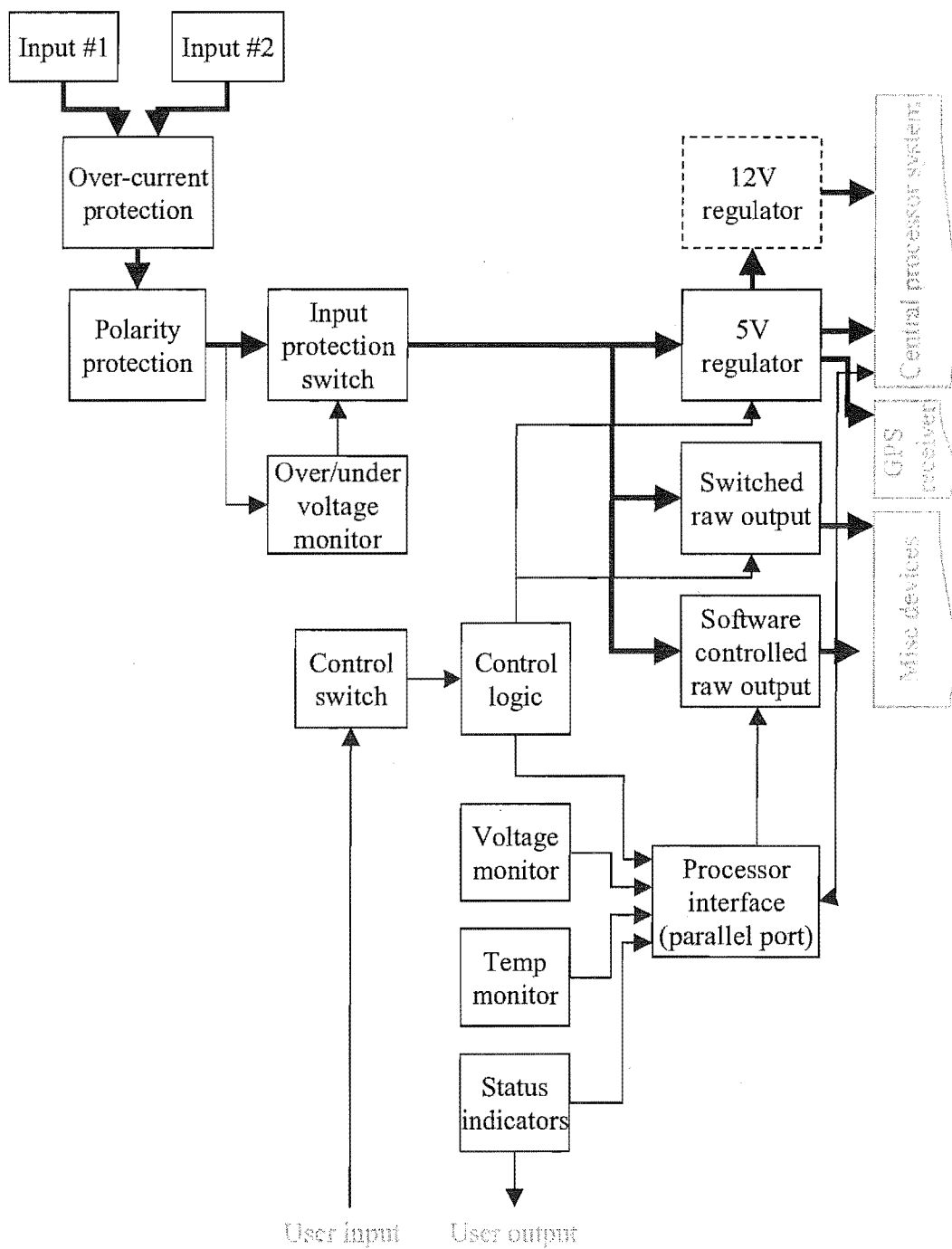


Figure 35, Block diagram of power supply subsystem hardware

The designs of the individual sub-components are then described. Each sub-component's design process includes the identification of the best components, a description of how they well interact and a circuit diagram of the completed sub-

components. At the conclusion of the sub-component design process, a circuit of the entire subsystem is presented.

Because the design uses switching regulators, the construction of the subsystem and in particular, the PCB layout, needs careful consideration. This is described in section 7.5 of [73] and includes an image of the final product, as shown in Figure 36.

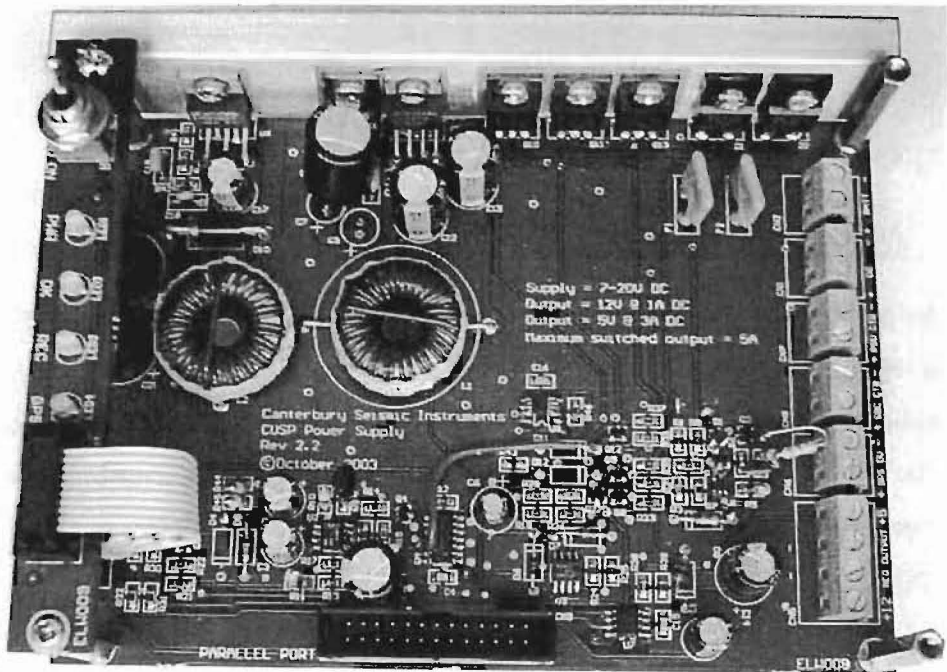


Figure 36, Photo of completed power supply subsystem hardware

9.2.7 Software suite subsystem development

The software suite subsystem represents a significant portion of the development effort for the CUSP System. This process is described in section 8 of [73]. This section begins by recognising two important differences between this project and previous work done by the author. Firstly, the flexibility and processing power offered by the use of a generic operating system and the x86 platform means that many previously-difficult seismograph features are now possible. Secondly, the author's inexperience with the Linux operating system means that it is impossible to formally describe the software system in advance. These two factors make a strong case for veering from the traditional approaches for software engineering, which

require detailed design documentation before implementation (such as the waterfall model or the unified process), to the relatively new methodology of the 'agile' approach [74].

Agile programming techniques are based on the four values [75]:

- Individuals and interactions over processes and tools
- Working software over comprehensive documentation
- Customer collaboration over contract negotiation
- Responding to change over following a plan

It is the last of these four values that applies particularly to this project, where the lack of knowledge of both the desired end result and the processes to realise them makes the traditional approaches unfeasible. Crudely put, agile methodologies do not rule out the 'try-and-see' approach as a means of defining goals, meeting customer requirements and finally providing a refined final product [76]. However, because the agile method's lack of formal specification may result in an inefficient or unreliable product [77], the approach is modified for the CUSP System to use the agile technique until a working prototype is realised, then to formalise the data structures and inter-application communications etc. This results in both a rapid development cycle and a highly reliable and maintainable software system.

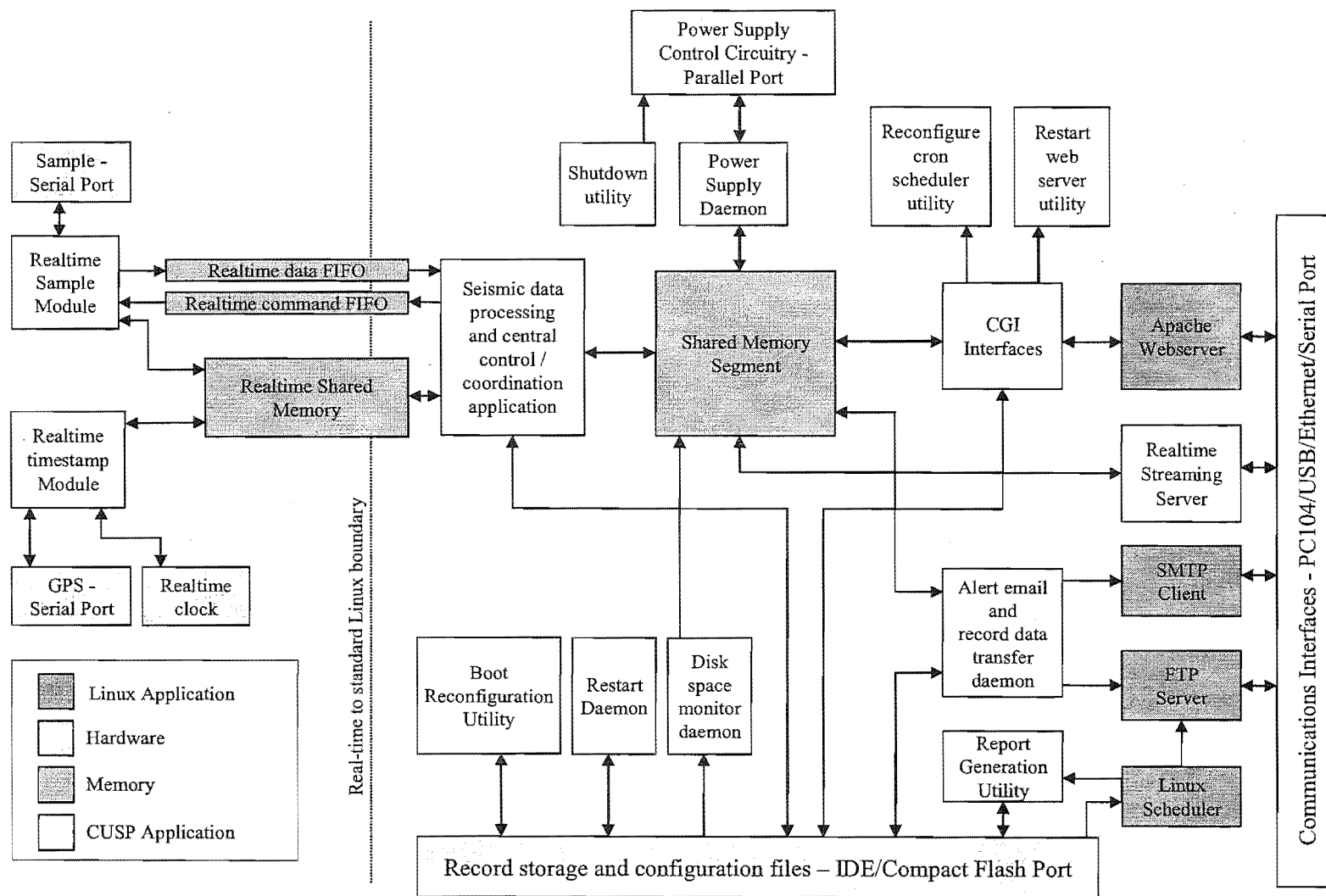
Once this new approach is described, the high-level requirements derived from the earlier chapters of this thesis are presented. The approaches to realise them are then estimated and the software suite subsystem broken into modular applications. These are then diagrammatically presented, showing the data paths between components and the interfaces to the hardware.

The system was next developed using the agile programming method and the results of this process are described. This review process indicated that, by using the approach of the generic OS and the x86 platform, many previously difficult-to-provide features were easily incorporated into the CUSP System. These include; the addition of FTP, Rsync and SSH servers and clients for command and file transfer,

the addition of lower sample rate options, and the real-time streaming of seismic data over the Internet. Furthermore, the initial prototyping indicated the best division points between modules to reduce areas of function duplication and to limit access to hardware, thus improving efficiency, reliability, maintainability and portability. The advantages of using shared memory segments and configuration files were also shown.

The results of the agile programming phase of the requirements development conclude with a module map, presented diagrammatically in Figure 37, and the definition the both the volatile and non-volatile data structures that are required for inter-module communication and instrument configuration.

Figure 37, Software suite subsystems components and interaction to hardware interfaces



Section 8.3 of [73] presents the formal definitions of the modules, as shown in Figure 37, and includes all input and output from the applications, including hardware, interprocess, configuration-file and data-file based transfers. Also defined are all interactions with the operating system and commercially available applications or utilities.

Section 8.4 of [73] describes the interprocess-communications data structure. This is followed by the definition of the non-volatile configuration files in section 8.5 of [73].

The largest section of [73], 8.6, describes the operation and development of the modules and applications of the software suite subsystem. The section begins by describing the development environment, including the programming language. The code common to many modules is then developed, forming a library of functions specific to the CUSP System. This helps ensure that any modifications result in consistent changes to all affected applications. The real-time applications are then described, followed by the application specific to the acquisition, analysis and storage of seismic data and overall control of the CUSP System. The daemons responsible for low-level control or functionality of the CUSP System, such as the real-time data-streaming server or for sending emails when a low battery state is encountered, are next described. The user interface is presented and begins with a description of the commercial web-server and the SSL security patch. The CGI modules are then described along with the interface web pages they support and their interactions with the remainder of the software suite subsystem. The section concludes with the description of the development of the scripts required to adapt the Linux operating system to the CUSP System and a description of the miscellaneous utility applications needed for various specialised tasks of the software suite subsystem, such as the health report file generator and a utility which rebuilds any corrupted configuration files at boot time.

The development of the software suite subsystem concludes with the description of a utility for a Windows-based PC that allows viewing of CUSP System records and conversion of the records to text, Matlab or Kinemetrics 'volume 1' files.

9.3 Final Specifications

The following sections describe the final specifications of the components of the CUSP System.

9.3.1 Sensors

Type	Three orthogonal MEM silicon accelerometers Temperature induced offset correction Axial misalignment correction
Range	$\pm 3g$
Sensitivity	<2 mg RMS noise floor (80Hz Bandwidth) <1.5 mg RMS noise floor (40Hz Bandwidth)
Dynamic range	69 dB (80Hz BW) 72.5 dB (40 Hz BW)
Mounting	Internal sensors Optional external mounting for borehole or array use Can utilise LAN wiring for complete building monitoring without additional cabling
Sampling	Zero jitter, zero skew autonomous sampling

Anti-Alias	8th order elliptic synchronised switched capacitor anti-alias filter ($f_c = 2 \times$ measurement bandwidth (BW)) Extremely high linearity over 0-100 Hz range
Sampling rate	800Hz
Conversion	16bit data conversion

9.3.2 Sample Signal Processing

Filtering	FIR digital anti-alias filter/decimator Perfect linearity
Measurement Bandwidth	40 or 80Hz
Recorded dynamic range	108dB (80 Hz BW) 108dB (40 Hz BW)

9.3.3 Processor

Type	Low power x86 based
OS	Multi-tasking real-time Linux based

9.3.4 Timing

Type	Low power GPS (standard)
Accuracy	Better than 400µs of UTC
Network	Potential use of network timing for reduced cost

9.3.5 Communications

Type	HTTP web server, FTP, Telnet, SSH, Rsync Email on Event feature LAN, Dial-up Server/Client, Serial link, Cellular Modem, Wireless/Bluetooth
Protocol	TCP-IP, SSL
Data integrity	Password security to instrument setup/data with general and admin user accounts
Features	Remote configuration of all parameters including IP number, Instrument setting, Power management etc Data retrieval Diagnostics

9.3.6 Triggering

Type	STA/LTA AND or OR filtered level detection
STA/LTA	Independent thresholds on each channel Selectable channel AND or OR triggering Thresholds adjustable from 2:1 to 200:1
Level	Independent thresholds on each channel Selectable channel AND or OR triggering Selectable lowpass, highpass and bandpass IIR filters or no filtering Level from 4mg to 4000mg in 1mg steps
Pre-event length	10 to 60 seconds in 1-second steps
Post even length	10 to 60 seconds in 1-second steps

9.3.7 Storage

Type	Removable Compact Flash card Unique record filenames PC readable
Storage time	Minimum 55 hours @ 200 samples/s No fixed upper limit – depends of Compact Flash size

9.3.8 Power

Supply voltage	10 – 24V DC
Power consumption	10 W typical 15W max
Supply monitoring	User selectable low voltage shutdown and auto re-power on resumption of power

9.3.9 User Interface

Type	Web browser based CGI scripted for advanced interactivity Platform independent Linux/Windows/Mac Can be configured / interrogated from any cyber-café in the world Secure Apache web server
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9.3.10 Environmental / Casing

Type	High strength aluminium
Protection	Spash-proof.
Ambient temperature	-10 to +70°C
Humidity	0 to 100% (non condensing)
Mounting	Central bolt between three spiked feet

9.4 Testing the CUSP Instrument

To validate a design, the final product must be checked to verify that it does what is asked of it in the design brief, and that its performance matches that of the final specification.

This section begins by testing the hardware performance, on a subsystem basis, against the specific values presented in the final specification. Exercising the entire system in a manner that covers the desired performance, defined in the design brief, tests the functional performance. Because the software suite subsystem components are tested individually during development, the software suite subsystem is included in this functional testing. The section concludes by discussing the results of the testing process.

9.4.1 Central processor subsystem

As the central processor subsystem consists of COTS hardware and a generic operating system with commercial packages, this subsystem's electrical and software testing is beyond the scope of this research project; the SBC is assumed tested by the manufacturer, while the Linux operating system is considered tested by the user community. Thus, the segment covering the functional testing later in this section is considered sufficient for testing of this subsystem's function.

9.4.2 Data acquisition subsystem

9.4.2.1 Signal path through hardware

The magnitude and phase response of the analogue data path was measured between the output of the accelerometer (removed for the test) and the input to the A/D converter. The test was performed with the parameters and instrumentation as shown in Table 17.

Table 17, Data acquisition subsystem signal path test parameters

Source	HP33120A 11MHz Function/Arbitrary Waveform Generator
Measurement	HP 35665A Dynamic Signal Analyser
V_{source}	1.8Vp-p
V_{offset}	+2.5VDC
Waveform	Sine

The phase change between the input and output signals, as well as the gain through the system, were measured by manually sweeping the frequency of the signal generator across the measurement band, and recording the input and output signals. The resulting gain and phase information is plotted and shown in Figure 38. Note the different frequency scales of the two plots.

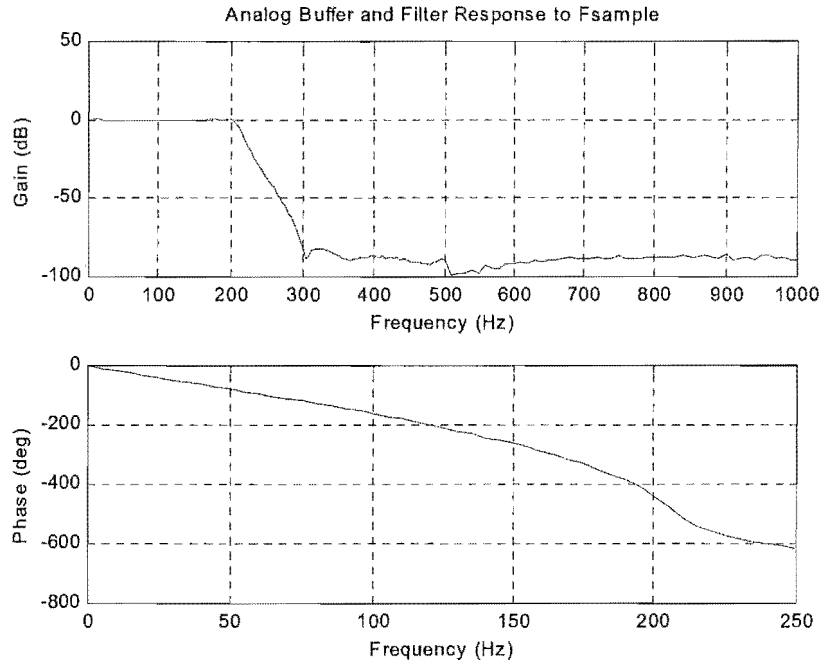


Figure 38, Data acquisition subsystem gain and phase response

Figure 38 verifies that the analogue signal path is within the specifications. The resulting phase error is less than $\pm 1.5^\circ$ and a gain error of less than $\pm 0.3\text{dB}$. The noise floor of the analogue section was measured as exceeding 78dB below the maximum signal amplitude, providing a 6dB margin of safety above the minimum required dynamic range.

9.4.2.2 Sample rate and jitter

The ‘jitter’ in the sample rate is the deviation from precisely periodic sampling, and has a serious effects on the effective signal to noise ratio (SNR). The formula for the calculation of the maximum possible signal to noise ratio in the presence of sample rate jitter is given in equation 14 [78] as:

$$SNR_{JITTER} = -20 \cdot \text{LOG}_{10}(2 \cdot \pi \cdot F_{IN} \cdot \tau_{JITTER})$$

where

F_{IN} = maximum input frequency

τ_{JITTER} = rms jitter in seconds

14

The jitter observed in the sample clock of the data acquisition subsystem¹⁴ is shown in Figure 39. The greyed portion of the figure shows the observed range of sample times when triggered on the previous acquisition start signal i.e. inter-sample time variance or jitter.

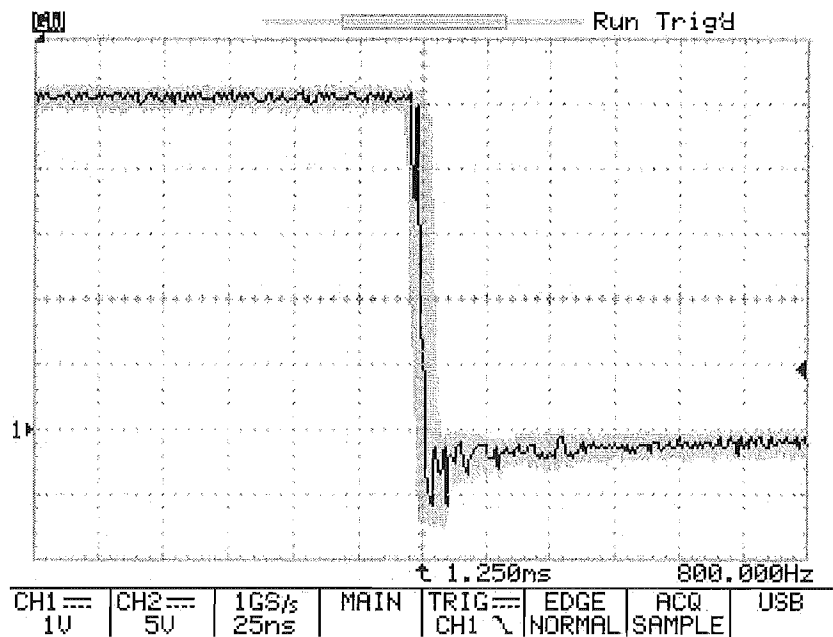


Figure 39, Observed sample rate jitter on chip select pin of A/D converters

With a worst-case RMS jitter of 10ns RMS (which is conservative, Figure 39 shows a maximum peak-to-peak of 10ns) and a maximum of 100Hz input signal (again conservative) the SNR limit due to jitter is then 104dB. Given that the specified noise floor is 2mg RMS over a $\pm 3g$ range, the maximum SNR of the CUSP System is 70dB. Therefore the jitter induced SNR limit is negligible.

The accuracy of the sample rate determines the accuracy of the records timing and more critically, the accuracy of any frequency domain analysis. Figure 39 shows a sample rate frequency of 800.000Hz, which implies an accuracy greater than 1 part per million.

¹⁴ Signal at the ‘chip select’ inputs to the A/D converters, at which time the converter starts its conversion routine.

9.4.2.3 Temperature correction interpolator

To test the routine in the data acquisition subsystem that interpolates the missing values in the reduced-size offset correction array, the correction array was replaced with linearly stepped data points. By substituting the standard indexing variable, the temperature, with an incremental variable, and constraining the A/D data with a fixed value, the output should now become a ramp, with the missing values in the stepped array correctly interpolated. The seismic data processing application was temporarily modified to allow the recording of non-filtered data to prevent the FIR anti-alias filter from averaging, and hence masking, any lost sample.

Figure 40 shows the output recorded when the interpolator is forced to increment in a step manner. The figure also shows that the correction period of the removal of the temperature dependant offset occurs at 150 corrections per second. This means that the digital antialias filter will filter any output steps introduced by the offset removal process so that they are not folded back into the recorded data stream.

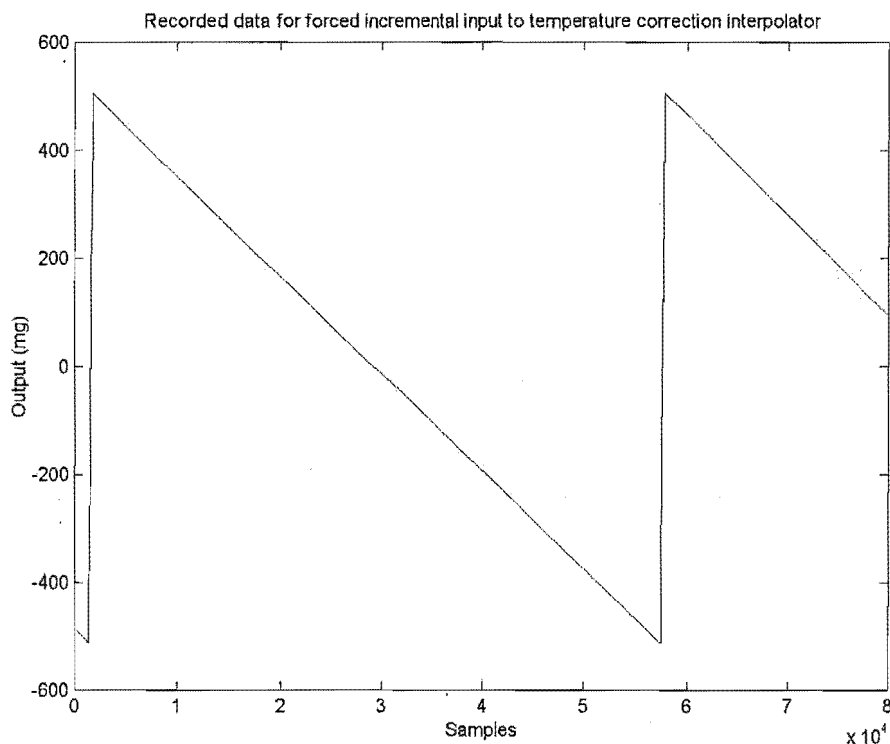


Figure 40, Operation of correction interpolator

9.4.2.4 Temperature correction performance

Testing of the correction process that removes the temperature induced offset was achieved by recording both the corrected and the raw acceleration data while the data acquisition subsystem was subjected to a temperature sweep. A magnified portion of the results of this test is shown in Figure 41, which clearly shows the effectiveness of the process. In the temperature section presented, the normalised raw acceleration changes from -13.5mg to $+15\text{mg}$, while the corrected output remains within $\pm 0.6\text{mg}$.

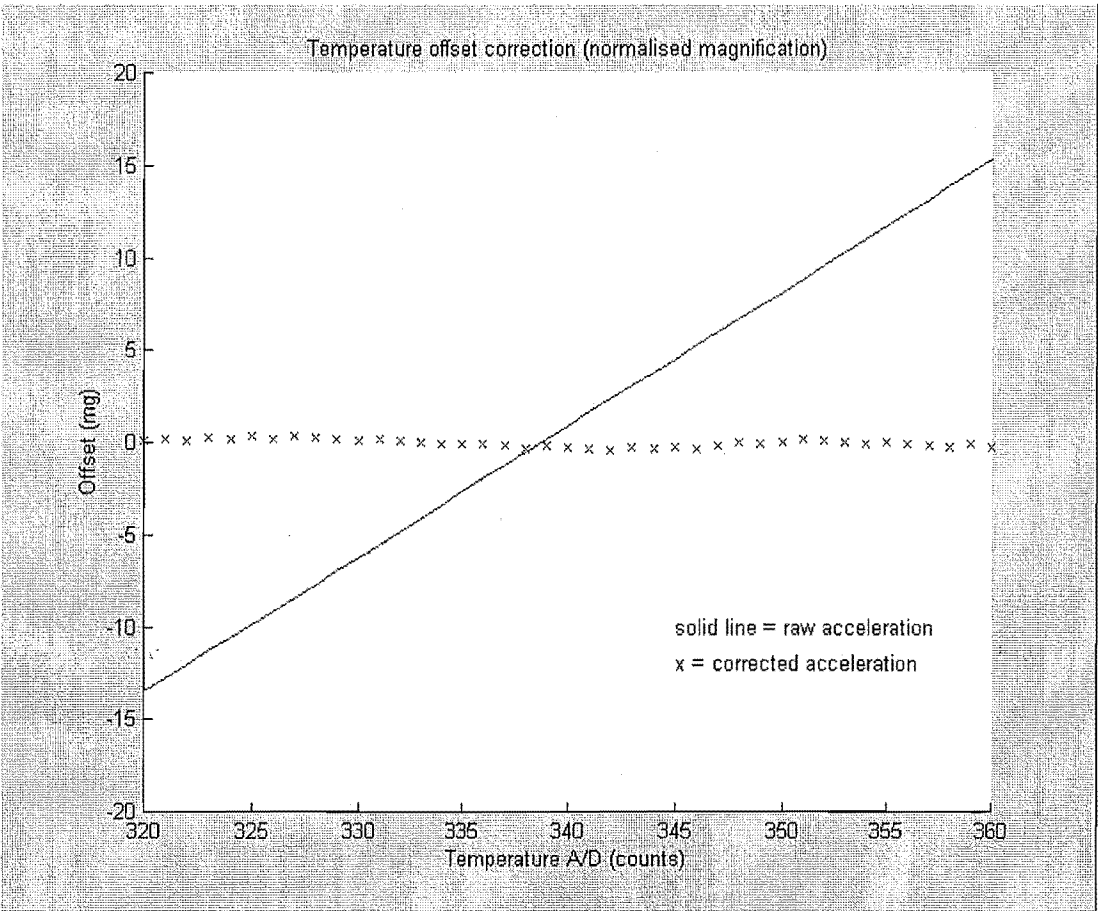


Figure 41, Magnified section of results of the testing of the temperature-induced offset correction routine

9.4.3 Power supply subsystem

The critical aspects of the power supply subsystem requiring testing are:

- The operation of the over-voltage and under-voltage safety mechanisms
- The efficiency of the circuits
- The short circuit protection
- The automated power on feature
- The quiescent current and,
- The output capacity

These aspects will be discussed in the following sections.

9.4.3.1 Operation of the over-voltage and under-voltage safety mechanisms

Applying a variable DC input to the PSU tests the operation of the over-voltage and under-voltage protection circuits. Applying a positive sweep and measuring the voltage at which switch-on occurs, and then applying a negative sweep and measuring the voltage at which switch-off occurs tests the hysteresis of the under-voltage cut off. These tests must be performed over a range of output loads to ensure consistent operation.

The results of the under-voltage protection circuit tests are shown in Table 18 and the over-voltage test results are shown in Table 19.

Table 18, Under-voltage protection circuit test results

Load\Test	1	2	3	Average	Hysteresis
2A @ 5V switch on	10.42V	10.36V	10.32V	10.37V	1.69V
2A @ 5V switch off	8.67V	8.72V	8.65V	8.68V	
1A @ 5V switch on	10.37V	10.38V	10.37V	10.37V	1.96V
1A @ 5V switch off	8.40V	8.45V	8.39V	8.41V	
0A @ 5V switch on	10.36V	10.34V	10.34V	10.35V	2.20V
0A @ 5V switch off	8.11V	8.15V	8.18V	8.15V	

Table 19, Over-voltage protection circuit test results

Load	Switch off voltage
2A @ 5V	24.8
1A @ 5V	24.8
0A @ 5V	25.0

9.4.3.2 Efficiency of the circuits

The efficiency of the power supply is determined by the ratio of the output power to the input power. The efficiency test is to be performed on both the 12V and 5V outputs, with varying loads up to the maximum designed output capacity, and with a varying input voltage. The results of this test are shown in Table 20 and Table 21. This data is shown graphically in the efficiency curves given in Figure 42

Table 20, Efficiency of 5V output for 10, 15 and 20 Volt inputs

Load (A)	V _{IN} =10V Efficiency		V _{IN} =15V Efficiency		V _{IN} =20V Efficiency	
0.2	0.175	0.57	0.100	0.67	0.100	0.50
0.4	0.220	0.91	0.175	0.76	0.150	0.67
0.6	0.375	0.80	0.285	0.70	0.200	0.75
0.8	0.480	0.83	0.325	0.82	0.250	0.80
1.0	0.600	0.83	0.400	0.83	0.325	0.77
1.2	0.750	0.80	0.475	0.84	0.375	0.80
1.4	0.900	0.78	0.575	0.81	0.425	0.82
1.6	1.050	0.76	0.630	0.85	0.500	0.80
1.8	1.175	0.77	0.750	0.80	0.550	0.82
2.0	1.280	0.78	0.825	0.81	0.600	0.83
2.2	1.425	0.77	0.900	0.81	0.675	0.81
2.4	1.575	0.76	1.000	0.80	0.750	0.80
2.6	1.750	0.74	1.075	0.81	0.800	0.81
2.8	1.875	0.75	1.175	0.79	0.850	0.82

Table 21, Efficiency of 12V output for 10, 15 and 20 Volt inputs

Load (A)	$V_{IN}=10V$	Efficiency	$V_{IN}=15V$	Efficiency	$V_{IN}=20V$	Efficiency
0.2	0.350	0.69	0.225	0.71	0.175	0.69
0.4	0.700	0.69	0.450	0.71	0.375	0.64
0.6	1.050	0.69	0.700	0.69	0.500	0.72
0.8	1.450	0.66	0.925	0.69	0.700	0.69
1.0	1.900	0.63	1.200	0.67	0.900	0.67

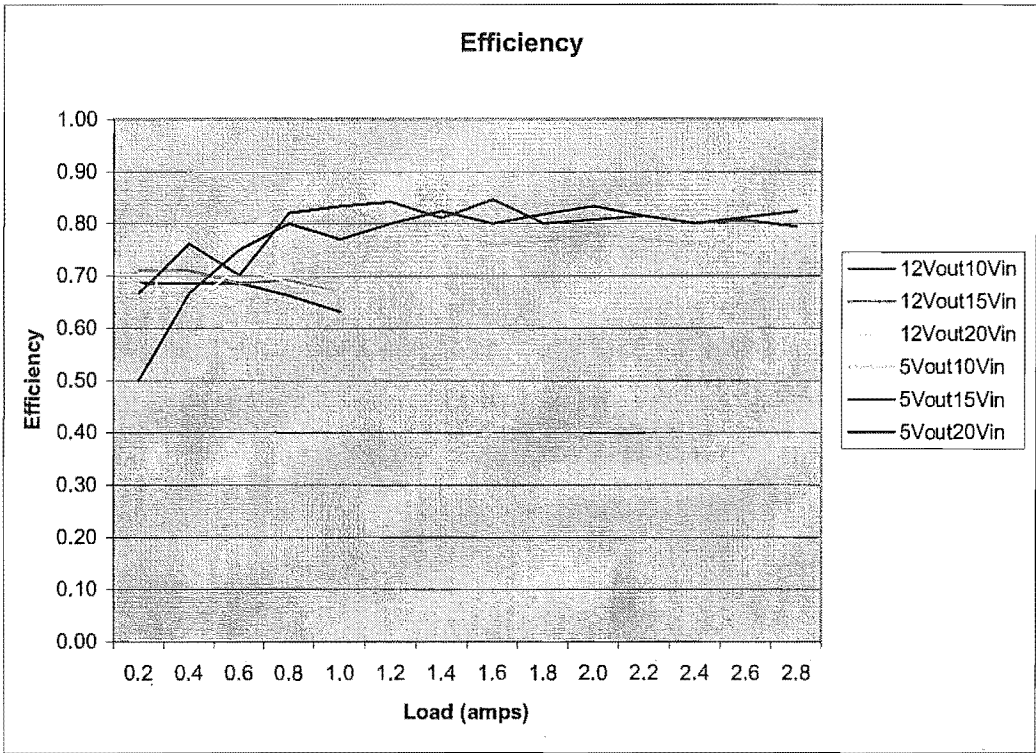


Figure 42, Efficiency curves for the power supply subsystem regulators

9.4.3.3 Short circuit protection

The short circuit protection ensures that the input current is limited to a safe value whenever an excessive output load is encountered. Short-circuiting the outputs of the 5V and 12V terminals tests the short circuit protection, and the results are shown in Table 22 and Table 23.

Table 22, Input current for short circuit on 5V output terminal

Current (A) with 20V input	0.70
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Table 23, Input current for short circuit on 12V output terminal

Current (A) with 20V input	1.00
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9.4.3.4 Automated power on feature

The switch-on voltage was measured at 14.20V during all conditions.

9.4.3.5 Quiescent current

The power consumption of the PSU when the system is detached from any load, and when switched off, determines the power loss of the system not attributed to efficiency loss. The current consumed with a varying input voltage, no load, and when both switched on and off is shown in Table 24.

Table 24, Quiescent current of power supply subsystem when on and off

Input voltage	Input current (mA) when off	Input current (mA) when on
4	0.9	0.8
6	1.3	1.3
8	1.8	1.8
10	2.2	2.2
12	5.6	25.6
14	6.5	26.5
16	7.3	27.3
18	8.1	28.1
20	8.8	29.3
22	9.6	30.5
24	10.2	31.6
26	4.2	4.2
28	5.5	5.5
30	7.3	7.3

9.4.3.6 Output capacity

The output capacity is the maximum output of the system before regulation is lost. This was measured by applying an increasing load until the output voltage dropped to 10% below the specified output voltage. The results are shown in Table 25.

Table 25, Output capacity test results

V in (V)	I in (A)	V out (V)	I out (A)
20	1.9	4.68	5.8
15	2.8	4.67	5.8

9.4.3.7 Results of testing

The results presented in the previous sections indicate that the power supply subsystem meets the desired design specifications. The 1.69V of hysteresis on the under-voltage shutdown indicates a good tolerance to high internal-resistance batteries, permitting the use of smaller batteries with a higher internal resistance.

The output capacity tests indicates that the system will remain in regulation until the maximum output is reached, at which point the internal current-limiting of the regulators will activate.

The efficiency of the 12V regulation circuit is better than expected, while the efficiency of the 5V regulator shows a drop in efficiency with lower output currents and higher input voltages. Because a typical SBC for the CUSP System will draw around 1-2 amps at 5 volts, this is not anticipated to be a problem.

9.4.4 Time signal generation subsystem and time stamp real-time module

The hardware for generating the time signal is straightforward and no useful testing can be performed other than functional testing. However, the overall testing of the software suite subsystem's real-time timestamp module and the time signal generation subsystem can be performed simply. The 1 Hz signal generated by the COTS GPS receiver is the master timestamp signal for the CUSP System. Provided that the system acquires this signal in the sample time stamping module within the specified $\pm 10\text{ms}$ of UTC (section 3.2.3) then the system meets the timing requirement.

The test is performed by temporarily modifying the real-time timestamp module to toggle a hardware line when the interrupt routine driven by the 1PPS signal is processed. Figure 43 shows the typical latency in the processing of the 1PPS signal interrupt service routine (ISR). Figure 44 shows the worst-case results recorded over an interval of some 10's of minutes, during which time the processor was loaded above that which is possible during normal operation of the CUSP System (i.e. source code compilation and file system searching etc).

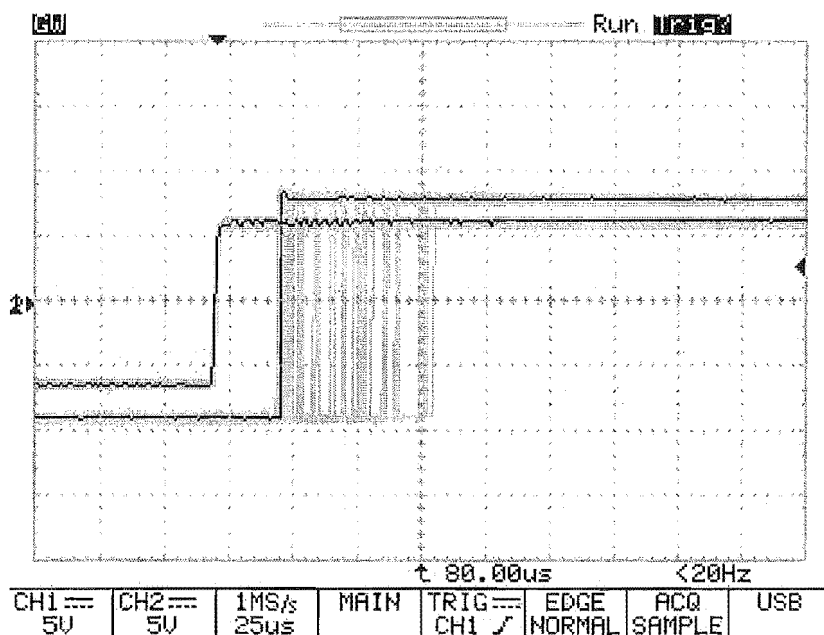


Figure 43, Timestamp latency - 1PPS GPS signal followed by timestamp ISR completion signal

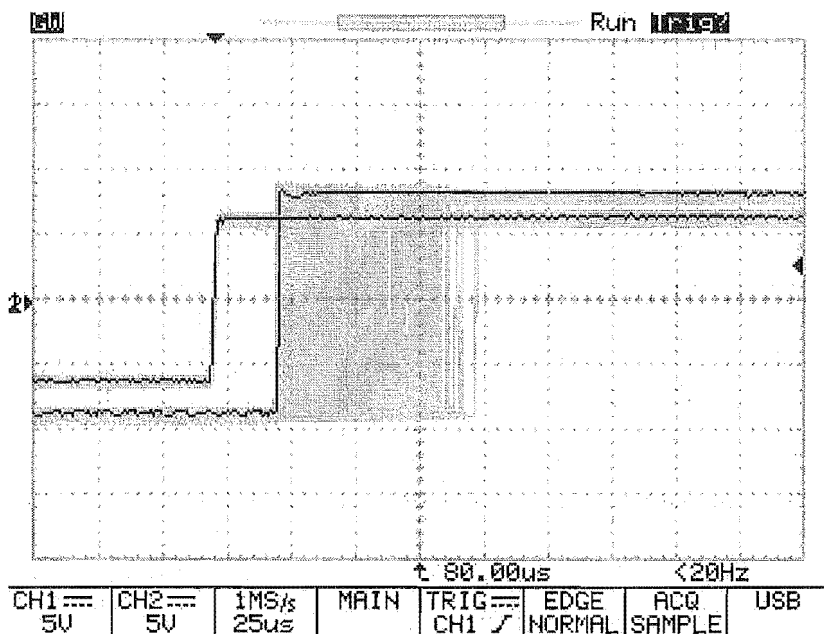


Figure 44, Worst-case timestamp latency - 1PPS GPS signal followed by timestamp ISR completion signal during heavy processing

The relatively high 85 μ s latency limit shown in Figure 44, while falling well within the maximum tolerable error, is due to the National Semiconductor GEODE processor core used for the CUSP System. The GEODE core uses a non-preemptable system-maintenance interrupt, which degrades the systems real-time performance.

9.4.5 Communications hardware subsystem

Because the communications hardware subsystem consists entirely of COTS hardware, the testing of this subsystems testing is beyond the scope of this project. It will therefore be included in the overall testing section.

9.4.6 Software suite subsystem

Given the quantity of software created, and the consequent number of test patterns required, the testing of the software suite subsystem presents a formidable task. Thankfully, because the CUSP System is an embedded system, the input parameters to most applications are well defined by the operating system, or by the software suite subsystem; thus, functional testing generally tests the software. The main risk for undefined operation arises from the ill-controlled user interface. The adoption of a common gateway interface (CGI) library, with built-in input conditioning, greatly restricts the potential for invalid input formats via this interface, but testing is still required for valid input ranges.

Because the software suite subsystem testing is an exhaustive process, detailed descriptions will not be provided. Generally, white-box testing was performed on the individual components of the software suite subsystem, while less formalised black-box testing has also been performed on the user interface, by opening it to public access.

While this testing is not as comprehensive as a fully structured test program, the lack of resources has limited to the testing time, and full third-party black-box testing is impossible. Thus, the acceptance of the correct operation of the software suite subsystem is to be derived from long-term operation of the CUSP System in a real-world application.

9.4.7 Overall functional testing

9.4.7.1 Noise performance of data conversion and processing system

The noise performance of the data acquisition subsystem and the digital anti-alias and decimation process can be determined by replacing the accelerometer with a dummy source of an equivalent impedance. The correction process for the temperature induced offset error must be stopped for this test to avoid step errors due to the phantom temperature changes. The test source is a voltage divider, consisting of two $100\text{k}\Omega$ resistors in series, connected between the transducers supply and ground pins, with the tap point at the transducers output pin. This provides an equivalent impedance of $50\text{k}\Omega$, which matches the transducers output impedance.

Figure 45 shows a manually triggered recording made with this test source in place. The measured output is $156\mu\text{g}$ RMS. This equates to a noise floor significantly lower than the 2mg output noise of the transducer [40]. Figure 46 shows the, essentially flat, noise frequency spectrum of the data acquisition process with the dummy accelerometer.

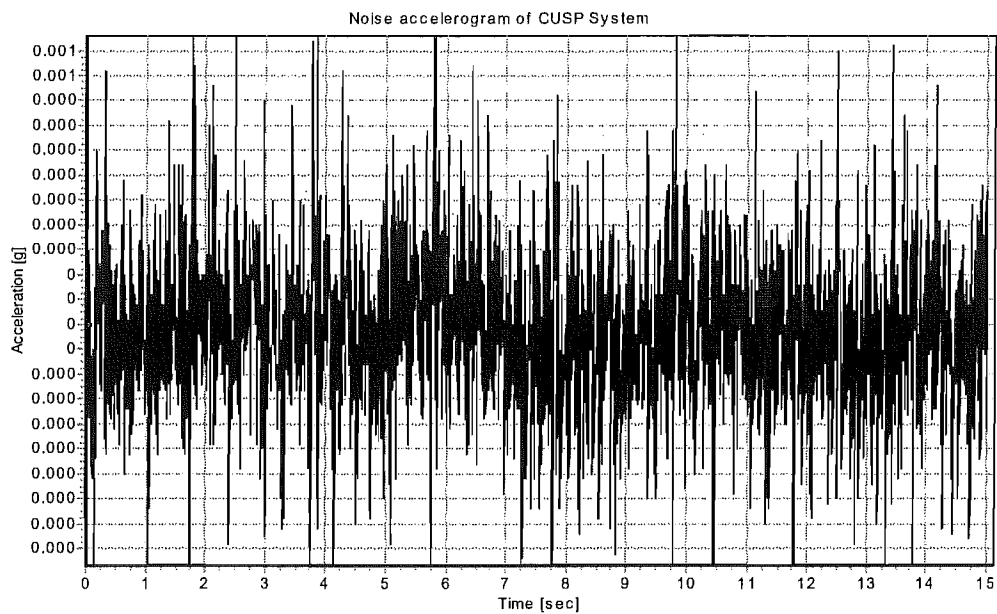


Figure 45, Noise accelerogram of data acquisition process with dummy accelerometer

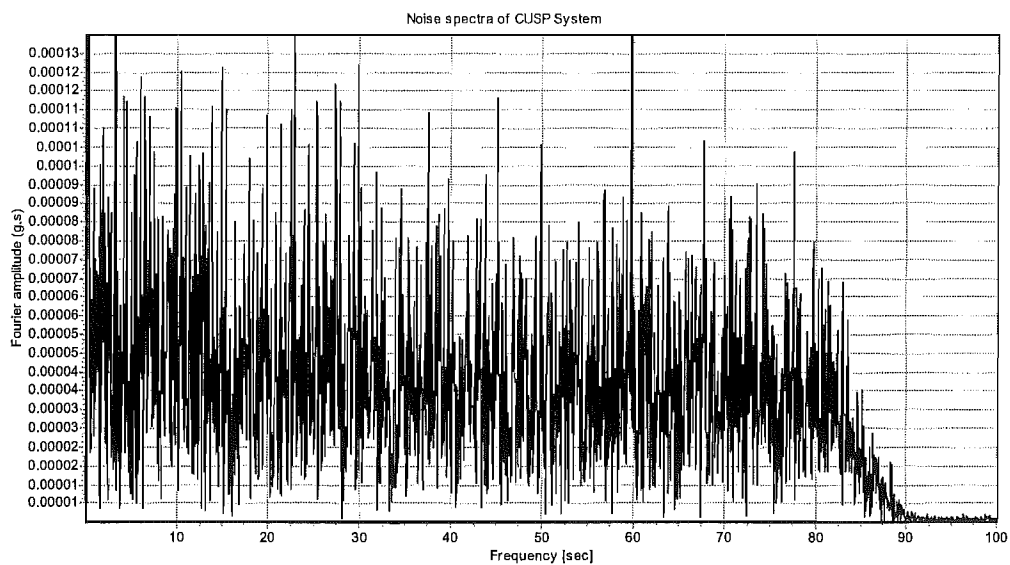


Figure 46, Noise spectra of the data acquisition process with dummy accelerometer

9.4.7.2 Noise performance of entire data acquisition subsystem

The noise performance of the CUSP System is difficult to ascertain due to the difficulty in ensuring a test location free from background seismic noise and cultural noise. The testing performed here can only be assured of highlighting any deviation from the expected output, which should lie somewhere between the transducer manufacturer's specified noise floor of 2mg RMS over a 100Hz bandwidth [40] and the results of the testing performed in section 9.4.7.1.

The tests were performed on a wooden table located on the second floor of a residential apartment block, adjacent to a building site. Figure 47 shows a manually triggered accelerogram of a typical channel. The RMS noise level determined from this recording is 1.92mg. Figure 48 shows the noise spectra for the same recording. As can be seen, the noise floor is essentially flat across the spectrum, and the amplitude rapidly drops off above the 80Hz cutoff frequency of the digital antialias filter.

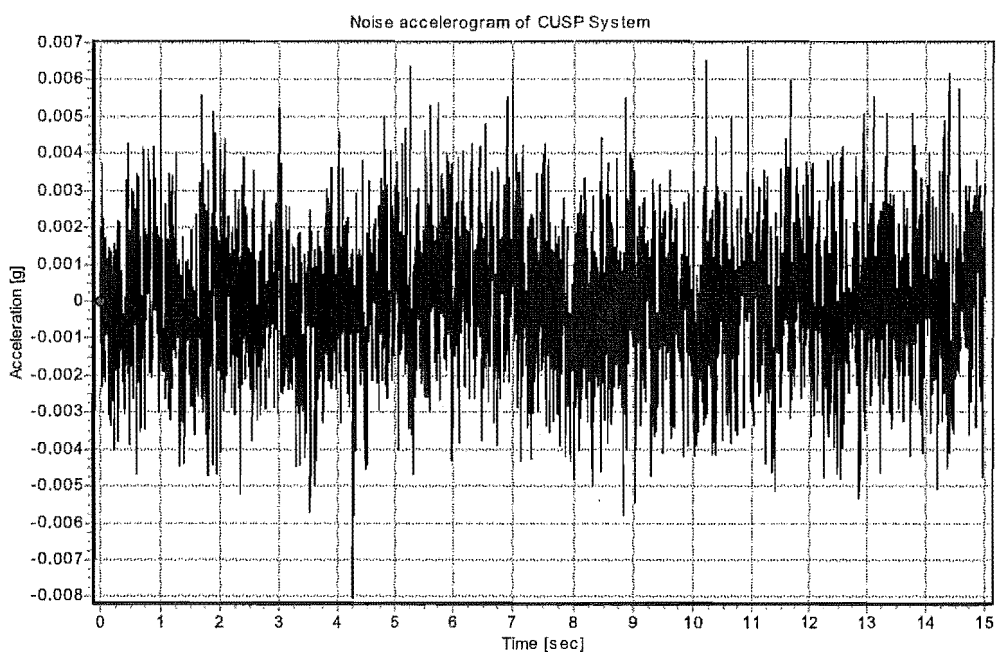


Figure 47, Noise accelerogram of data acquisition process with accelerometer

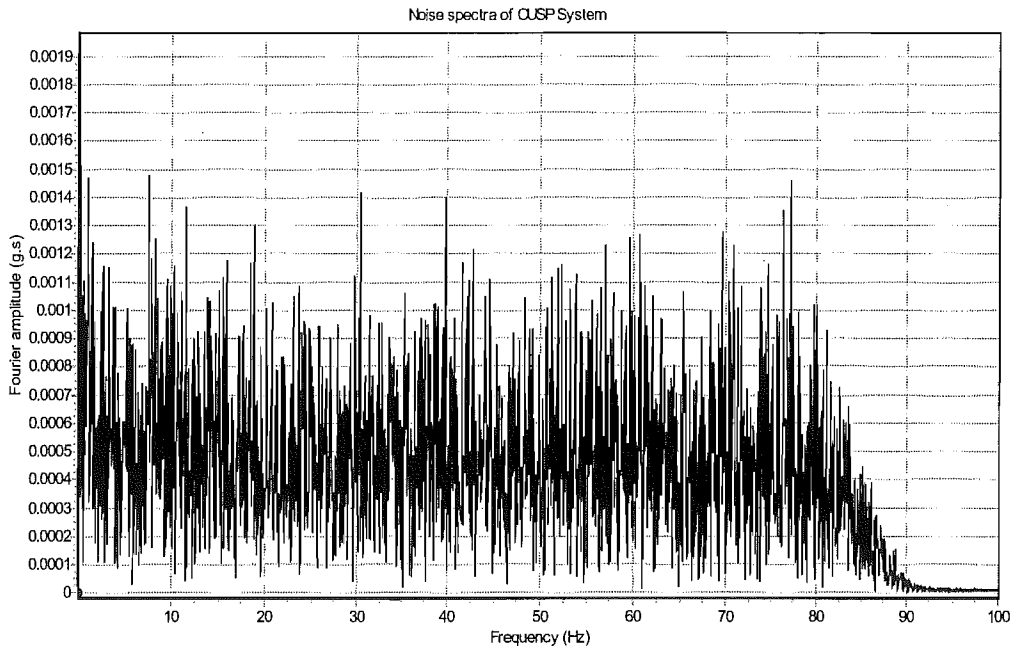


Figure 48, Noise spectra of the data acquisition process with accelerometer

9.4.7.3 Sampling

The loss of samples due to processor overload or software errors will result in a significant distortion to the signal. Therefore, it is critical that every sample for every sample interval is acquired, and, when necessary, recorded. Generating and recording a test signal with known parameters tests the sampling integrity. The known signal is generated by modifying the data acquisition subsystem hardware to provide a saw-tooth signal. This digitally-produced signal ensures that every sample can be tested, as slight mismatches in linearity or periodicity of an analogue source may result in false test results. The seismic data processing application was also modified to allow the recording of non-filtered data to prevent the FIR anti-alias filter from averaging any lost sample so that they would not be noticed.

The results of a 100 second test are shown in Figure 49. The test was performed with a high loading on the processor (simultaneous network activity, data streaming and directory function ('du -a \') plus with all the CUSP System daemons operational). As can be seen, no samples were missing during this test.

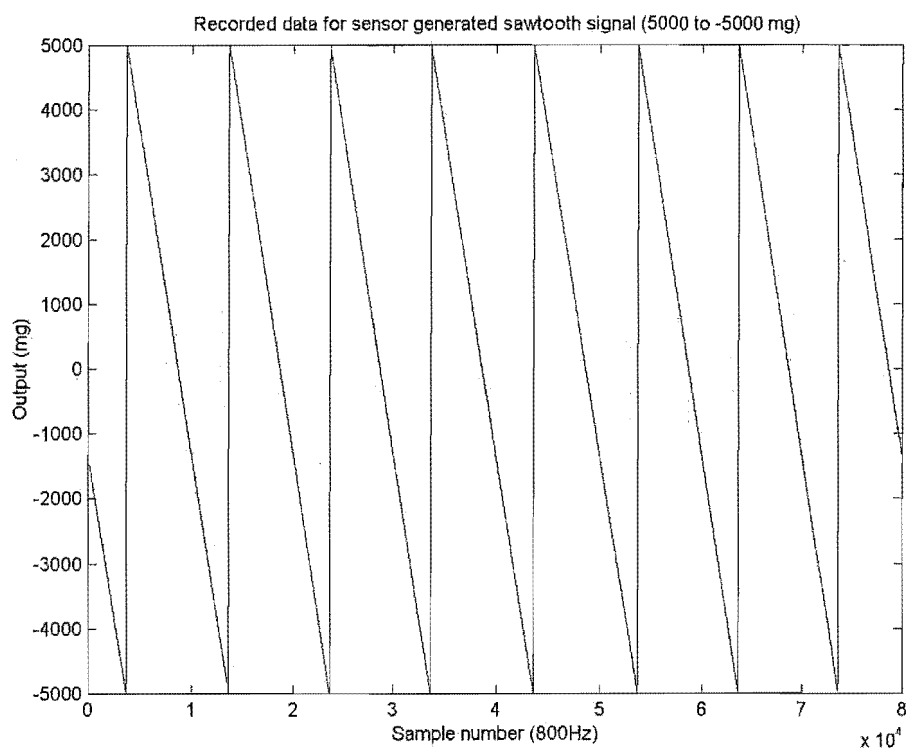


Figure 49, 100s test of data acquisition subsystem with saw-tooth signal input

9.4.7.4 Shake table testing

Shake table testing provides an excellent means of testing the fidelity of the recording as well as the triggering system. The shake table tests were performed on the Civil Engineering Department's shake table at the University of Canterbury. A Kinematics Etna was placed alongside the CUSP Instrument under test, along with a reference accelerometer. This configuration can be seen, with computer technician Peter Coursey, in Figure 50.



Figure 50, Testing the CUSP Instruments alongside the Etna on the shake table

Amongst the tests performed were the motions from the 1940 El Centro, California record and the 1996 Arthur's Pass, NZ, earthquake. The test records were attenuated due to the limitations of the shake table's control system.

Figure 51, Figure 52 and Figure 53 show the accelerograms of the attenuated 1996 Arthur's Pass event recorded by the CUSP Instrument, the Kinematics Etna instrument and the reference accelerometer respectively. Figure 54 and Figure 55 show the deviations between the CUSP Instrument and the Etna instrument from the reference accelerometer respectively.

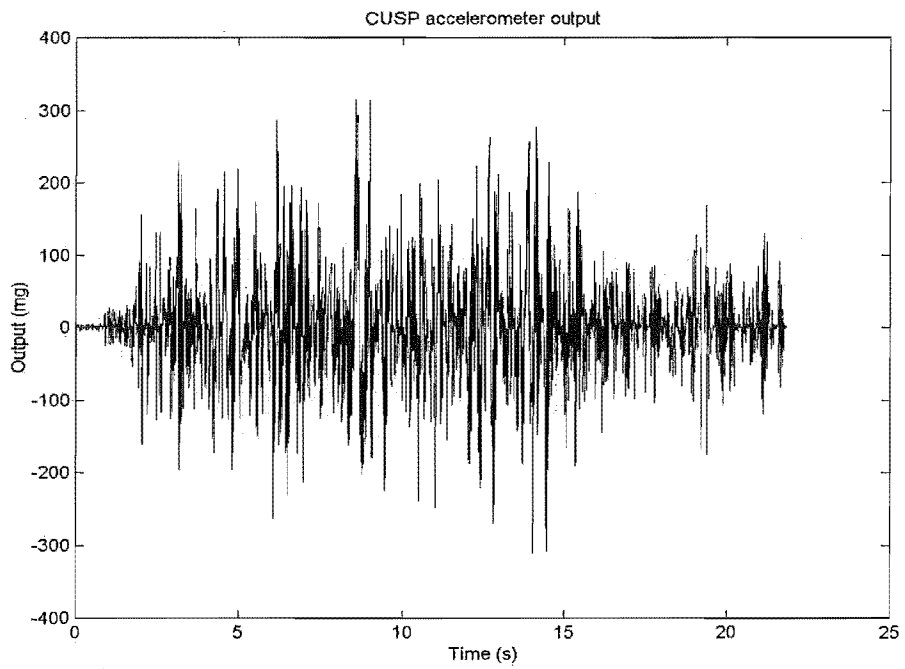


Figure 51, CUSP Instrument accelerogram of the 1996 Arthur’s Pass earthquake

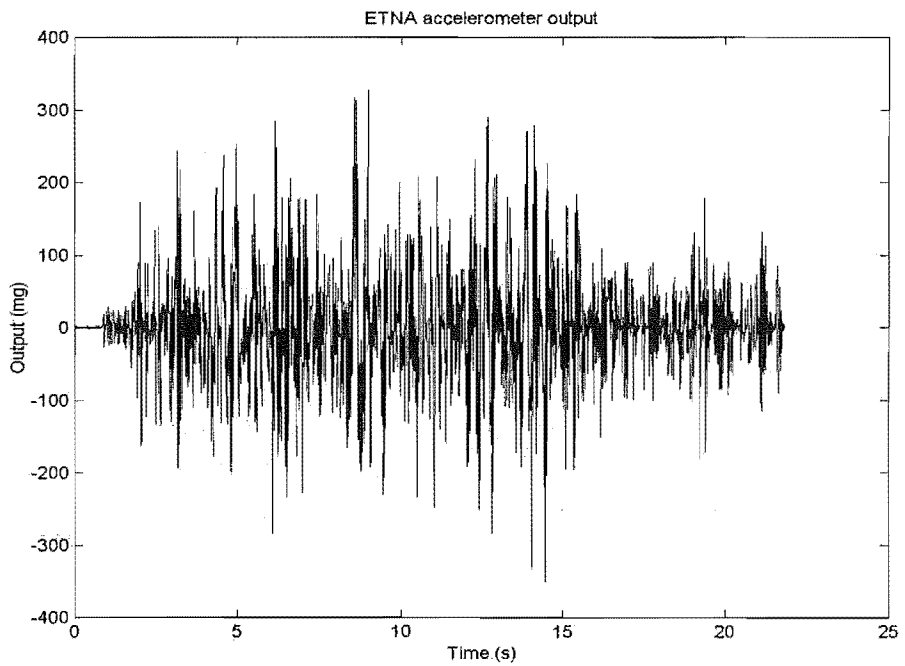


Figure 52, Kinematics Etna instrument accelerogram of the 1996 Arthur’s Pass earthquake

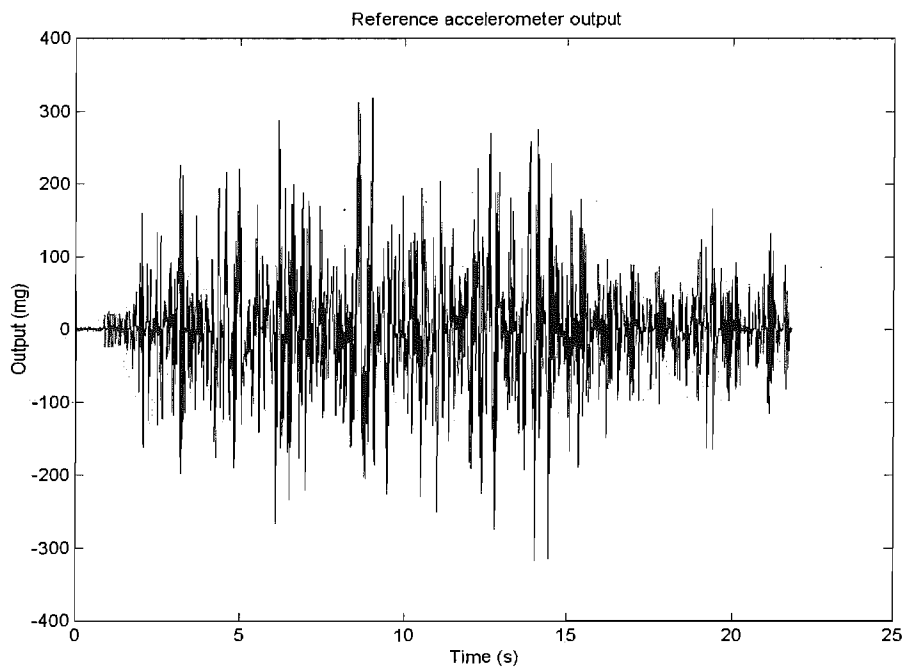


Figure 53, Reference accelerometer accelerogram of the 1996 Arthur's Pass earthquake

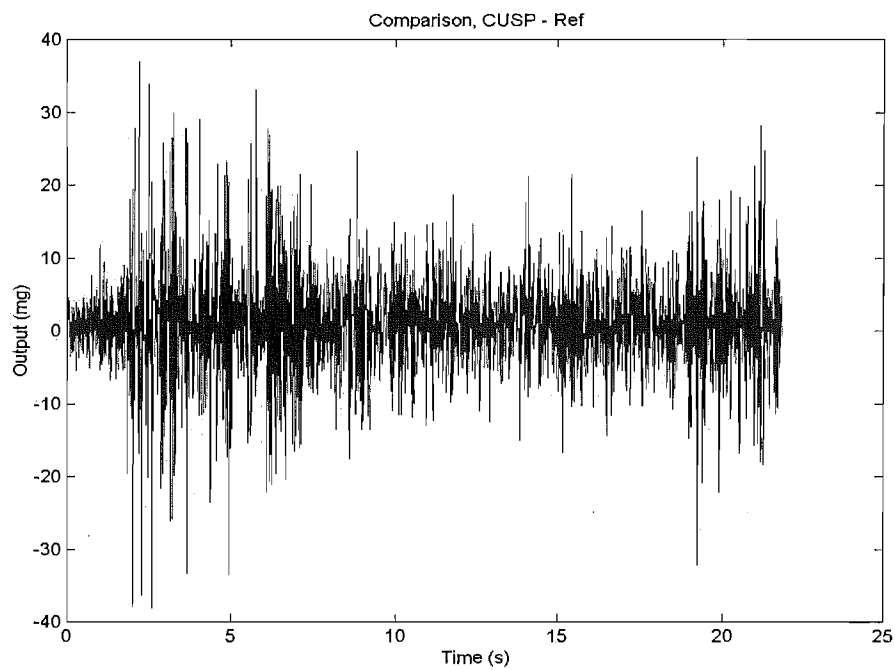
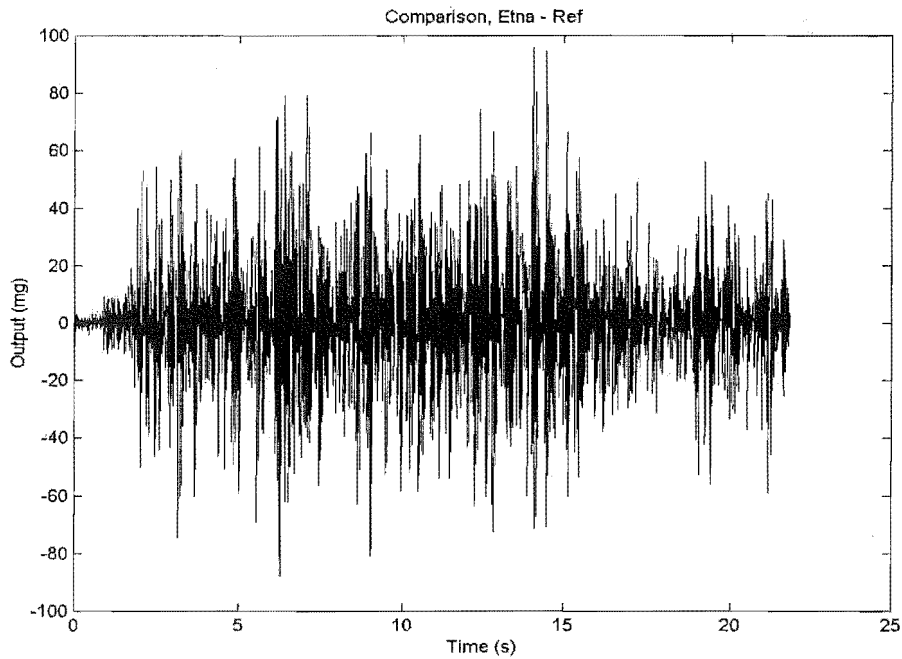


Figure 54, Difference between CUSP Instrument and reference accelerometers accelerograms of the 1996 Arthur's Pass earthquake



**Figure 55, Difference between Kinometrics Etna instrument and reference accelerometers
accelerograms of the 1996 Arthur's Pass earthquake**

The higher than expected deviation between the Etna and the reference accelerometer shown in Figure 55 may be due to a timing error in the Etna's sample rate, as shown in Figure 56 and Figure 57. These figures show the start and ends of the recorded event for all the instruments, from which, a clear deviation in the sample timing of the Etna is visible.

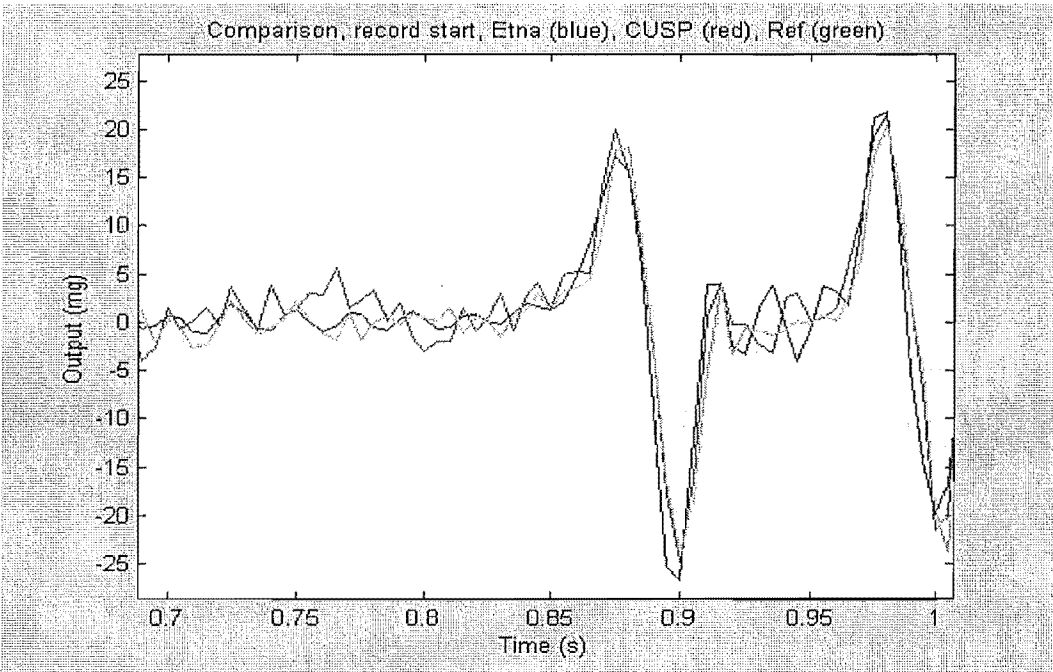


Figure 56, Start of Arthur’s Pass 1996 record for all instruments showing sample synchronisation

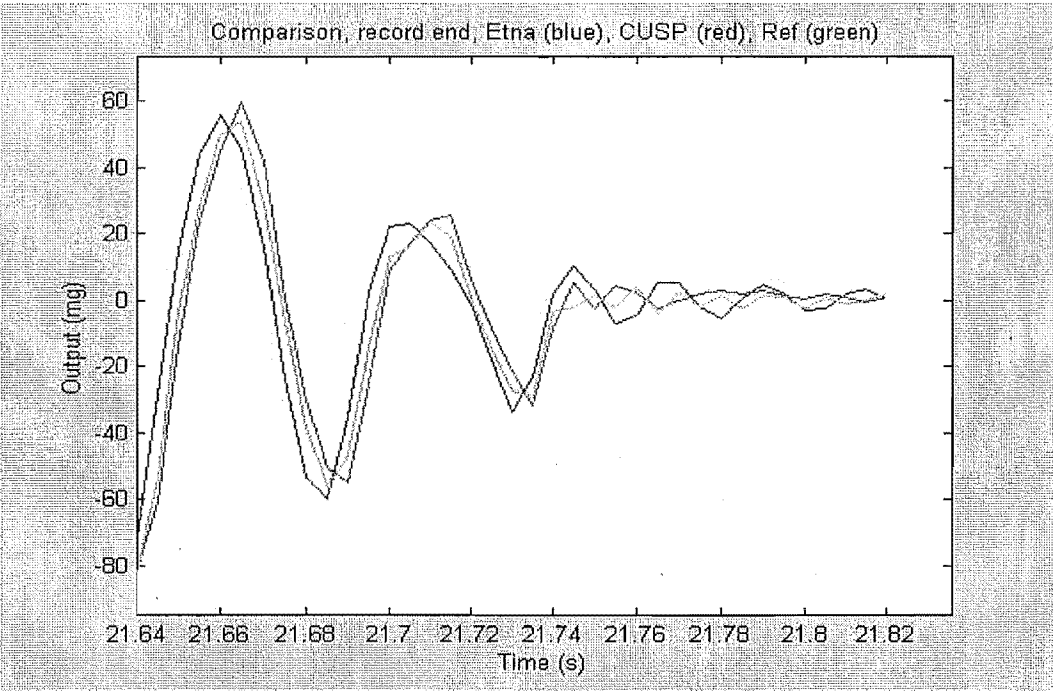


Figure 57, End of Arthur’s Pass 1996 record for all instruments showing loss of sample synchronisation in the Kinometrics Etna instrument

In order to determine whether the higher than expected deviation between the Etna instrument and reference accelerometer subtraction is due to the sample rate error,

frequency domain analysis can be used. Figure 58, Figure 59 and Figure 60 show the frequency spectrums of the three recordings. It is clear that the reference accelerometer utilises a higher sample rate from the lack of evidence of an antialias filter in the spectra.

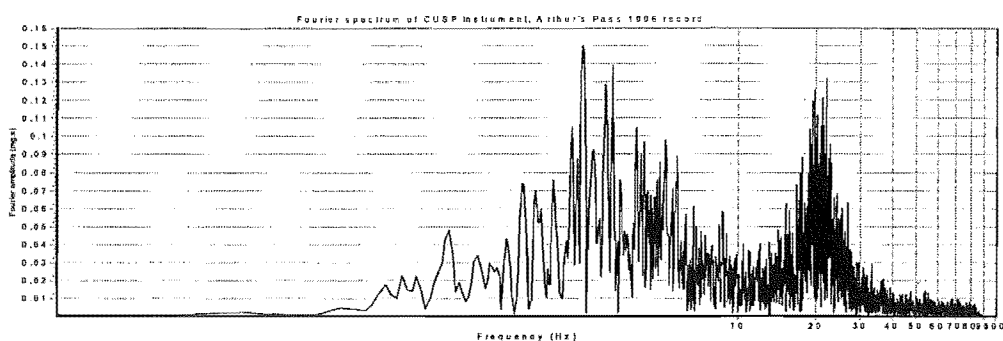


Figure 58, Frequency domain analysis of Arthur's Pass 1996 record for the CUSP Instrument

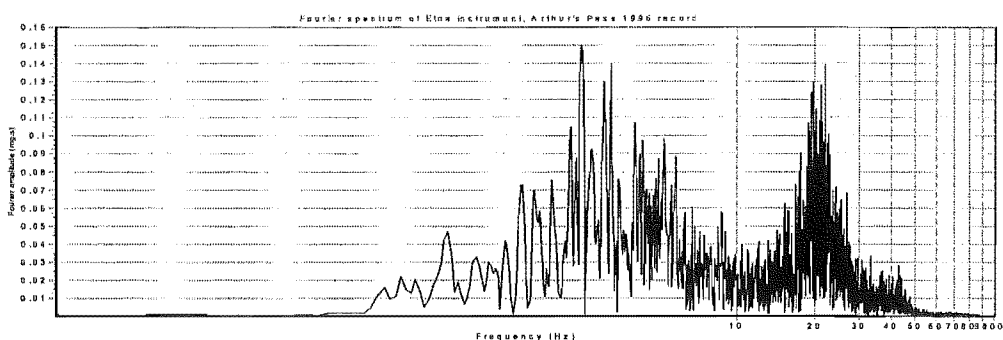


Figure 59, Frequency domain analysis of Arthur's Pass 1996 record for the Etna instrument

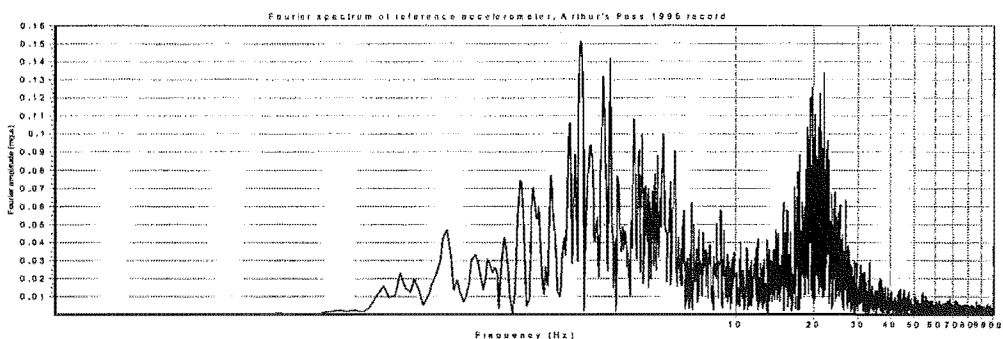


Figure 60, Frequency domain analysis of Arthur's Pass 1996 record for the reference accelerometer

All three spectra show good agreement, however, the Etna instrument exhibits a small deviation from both the reference and CUSP spectra at around 42Hz, and again at 55Hz. Also, the CUSP Instrument shows a small deviation at very low frequencies, which can be attributed to the $1/f$ noise discussed in section 8.4.1.1.

9.5 Conclusions

The test results show that the CUSP System meets or exceeds all of the design parameters.

The data acquisition subsystem has proven to effectively correct the temperature induced offset errors, maintaining a $\pm 0.6\text{mg}$ offset from a raw change of $\pm 14\text{mg}$. While this value may not be realised over long periods due to the fact that the offset can move within the eye of the offset's hysteresis loop, it shows the effectiveness of the interpolator, and the effectiveness of maintaining a stable baseline throughout the duration of a record. The noise floor testing of the combination of the data acquisition subsystem hardware and the signal processing performed by the software suite subsystem in the central processor subsystem shows the effectiveness of this approach. The basic noise floor of the data acquisition process is $156\mu\text{g RMS}$, well below the sensors noise floor of around 2mg RMS . This allows the current data acquisition circuit design to be recycled in the future if better transducers are released.

The timing performance is somewhat less than expected due to the relatively poor performance of the real-time Linux patch when operating on a Geode based computer system. While the maximum delay of $+85\mu\text{s}$ is within the specification (and considered very good for seismology), if this becomes an issue with certain applications, the low-cost Geode based SBC can be replaced with an equivalent Intel device, with which basic testing indicates much improved real-time performance.

The latency jitter in the timing process justifies the dedicated data acquisition subsystem processor, which has proven to limit the sampling jitter to 10ns RMS , which corresponds to a $\text{SNR}_{\text{JITTER}}$ of over 104dB .

The power supply subsystem tests show that this component of the CUSP System effectively fulfils its requirements. The PSU unit provides up to 3 times the required power allowing scope for using higher power processor platforms if required. However, the efficiency drops a little as the output load reduces, slightly reducing the overall efficiency of migrating to a low-power processor platform.

The software suite subsystem testing can not be considered conclusive of the performance of this component. Software systems cannot ever be proven error free and the continued use of the CUSP System will undoubtedly uncover errors. However, to the use of the Linux operating system (with its application containment) and the ability to communicate with the system remotely, means that the system will almost certainly not completely 'crash' and corrected applications can be installed remotely and easily.

The comparison between the CUSP Instrument, the Kinometrics Etna and the reference accelerometer on the shake table indicate the CUSP Instrument exhibits favourable performance. With respect to sample rate and frequency response, it enjoys superior performance, falling short only in the areas of dynamic range and low-frequency fidelity.

10 Results

10.1 Design process

The design process, presented in chapter 3, began with the traditional task of identifying the desired functions and performance and collating them into a simple design brief. Chapter 4 presented a review made of the instruments developed prior to instigation of this research project. This indicated the likely levels of performance required to achieve the goals of the design brief. Two critical design aspects were also identified by considering the lessons learnt from the design cycles of previous instruments, firstly, the correction of the low-cost MEMS accelerometers, and secondly, the problem of component obsolescence.

With the help of the previous design experiences, a discussion of the most effective means to realise the design brief's goals resulted in a design specification given in chapter 5. This outlined the design brief's goals in terms of what the implementation of the various requirements entailed.

In order to provide as much protection from component obsolescence as possible, a new approach was developed and described in chapter 6. The approach presented requires three key ingredients; COTS or other low-cost throwaway hardware, standard hardware interfaces between COTS components and a generic-type operating system. This creates a high-level design that does not depend on exact replacement modules, thus side-stepping the issue of individual or module component obsolescence. This new approach created a deviation from the typical development of a product, in that the design process now focussed more on the identification of module boundaries and the interfaces between them, rather than the means to implement modules. The modules and interfaces were specified in chapter 7.

Correcting the outputs of the low-cost surface micromachined MEMS accelerometers was discussed in chapter 8 after characterisation of the device chosen for the CUSP System. The sensors were found to exhibit two non-correctable characteristics;

thermally excited zero-point offset hysteresis and low-frequency $1/f$ noise. The hysteresis is not considered a serious problem for strong motion seismology, as the maximum rate of offset error change due to this error is slow compared to the duration of a typical strong motion recording. Unfortunately, even though the magnitude of the $1/f$ noise is small, it may result in poor displacement record fidelity. This is a fundamental limit of the instrument. Methods to correct for the other errors of direct thermal offset errors and the axial misalignment were discussed and solutions presented.

Because many of the component modules were COTS based, the implementation of the CUSP System was relatively straightforward and summarised in chapter 9. The data acquisition subsystem required careful design work to ensure that the required gain and phase linearity were provided. The software suite subsystem also presented significant design effort, but because of the buffering effect of the generic Linux operating system, maintenance and portability of this code are simplified.

In general, although the CUSP System is designed for a long service lifetime, the design approaches and processes described in this thesis have resulted in a low-cost system that provides an excess of performance and has required minimum development work.

10.2 Laboratory testing

Testing of the instrument on the shake table at the Civil Engineering Department of the University of Canterbury provided the ideal means to simulate real earthquakes. This was useful for testing the overall functionality of the instrument, such as triggering, as well as for testing the signal acquisition performance. The tests presented in chapter 9 proved the performance of the data acquisition and recording process, and the instrument compared favourably to the reference accelerometer and a Kinemetrics Etna instrument.

10.3 First record

The first record captured by a CUSP instrument was a M4.9 event with the epicentre located 40km northeast of Christchurch, NZ, where the instrument was located. The instrument was installed on the ground floor of the four-story Civil-Mechanical building at the University of Canterbury. An accelerogram of the recorded motion is presented in Figure 61, which shows a peak acceleration of 14mg, which is just above the limits of human perception.

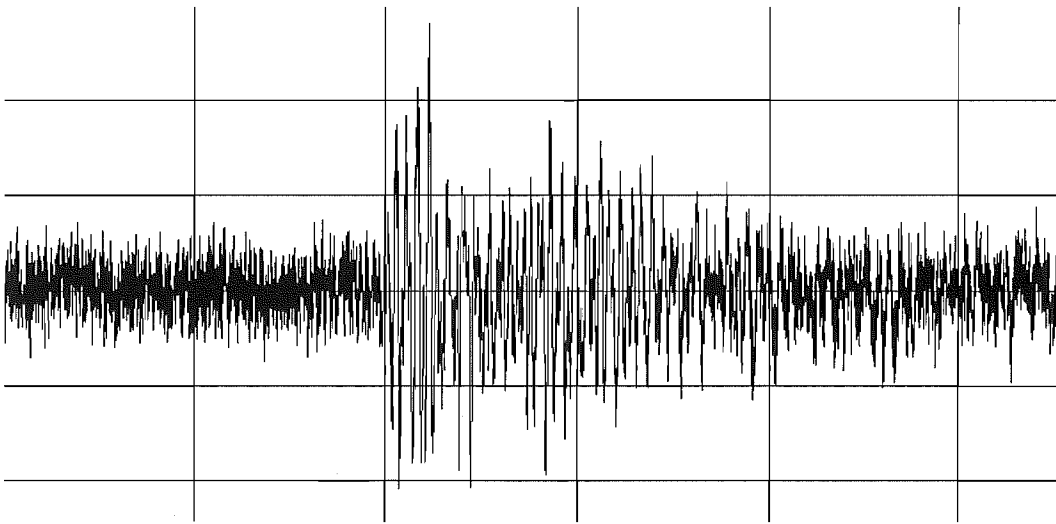


Figure 61, First event captured by a CUSP instrument

10.4 Use in engineering research

The CUSP System has been used for a structural engineering application. Dr. Bruce Deam of the Civil Engineering Department at the University of Canterbury has used the CUSP System as a data acquisition system for a student laboratory, which analyses a stairway that vibrates when used. The CUSP Instrument measures the frequencies and amplitudes of vibrations induced in the staircase allowing the students to design a tuned mass damper to reduce the vibrations. The instrument can be seen in Figure 62, located half way up the stairway on the far side.

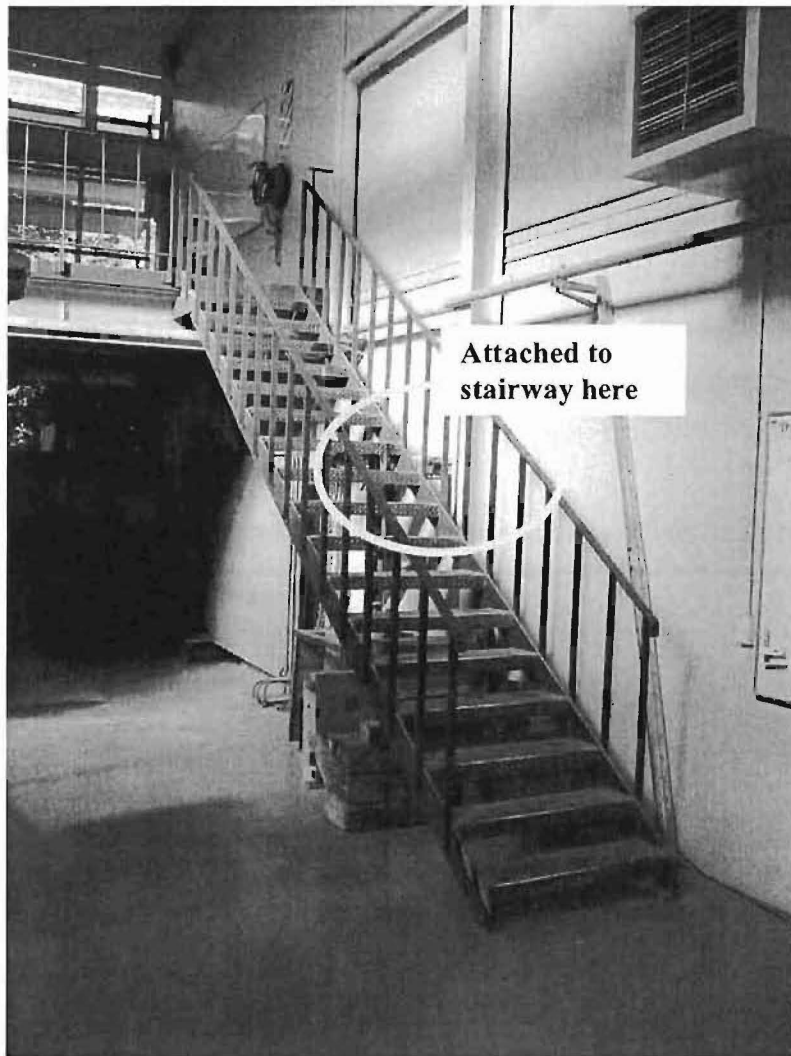


Figure 62, CUSP Instrument mounted on vibrating stairway (courtesy of B Deam)

10.5 User feedback

The first commercial user of the CUSP System has been the Geonet Project, operated by Geological and Nuclear Sciences, the New Zealand Crown Research Institute charged with, amongst other requirements, monitoring seismic activity for the government.

At the time of writing, the GNS have installed some 10 instruments inside and around the city of Christchurch, but as yet no events have been recorded. They have also

laboratory tested several early releases of the instrument, and their feedback has resulted in several modifications to the CUSP System. These changes were largely software modifications, such as the addition of a field allowing the modification of the network mask for connecting to other networks.

The GNS feedback has been positive, and, considering the market evaluation they performed before deciding to choose the CUSP Instruments, their confidence provides a verification for the design.

10.6 Merits of the modular approach

The value of the modular approach has already proven itself useful. Since the inception of the project, the CUSP System has been transferred from the desktop development PC to a first SBC and then another, improved, SBC. The first SBC was a National Semiconductor Geode 233 based design, requiring both 12 and 5V outputs, and providing only two communications ports. In this configuration, the third communications port for the modem interface was provided by means of a USB to serial port adapter. This technology was incorporated simply by means of adding the driver to the Linux kernel and configuring the operating system to redirect the serial communications via this adapter. No modifications to the CUSP Systems software were required. The transfer to a second SBC platform was made to capitalise on the reduced power consumption of the replacement system. This platform was again a Geode based product, but needed only a single 5V power source, and provided four communications ports. The adaptation to this change was simply to reconfigure the operating system to use the new communications port. In the interests of lowering the build cost, the components associated with the 12V regulator on the PSU were not populated in units built for this platform.

Other advantages of the modular approach have been proven with the design of a new range of transducers aimed at providing enhanced resolution. While these sensor systems are in the preliminary development stage, the merits of the chosen, scalable, interface have been proven in it's successful acceptance of the increased resolution data transfer.

11 Conclusions and discussion

The need for large numbers of strong motion accelerographs was established at the beginning of this thesis. Unfortunately for most research communities, the increasing performance of strong motion equipment, combined with a need for long service lifetimes, comes with an increasing cost. This results in lower than optimal instrument densities or reduced coverage areas. The CUSP System aimed to fill the gap in the market where acceptable performance and low cost coincide.

To reduce the cost of the instrument as much as possible, the goals of the CUSP System were defined by investigating the basics of ground motion data acquisition rather than by trying to offer the best performance or by developing specifications simply to outperform competitors.

Prior to the instigation of the CUSP System research project, several instruments had been developed by the author, which provided the benefit of experience. This experience indicated a major failing in the previous instruments, and indeed of the majority of commercially available products: component obsolescence. This problem either severely limits the service lifetime of a product, or inflates its cost out of proportion to the products performance. Unfortunately for seismic monitoring applications, the high performance required limits the effectiveness of traditional approaches to dealing with component obsolescence when attempting to retain a low initial and ongoing maintenance cost.

A new approach was sought that provided an effective solution to component obsolescence for low-cost but complex applications. The approach that this thesis presents is the creation of a system of COTS, or otherwise low-cost, disposable modules, connected in hardware by industry-supported, standardised, interfaces, and in software by a generic operating system. This places the system design and development at a much higher level than traditionally used and results in a system tolerant to changes to the component subsystems, the designer then has only to contend with obsolescence of architectures and interfaces. The generic operating system further shields the design from the effects of changes of hardware components.

This new approach presents a novel solution to the first of the fundamental problems this research sought to address – designing low-cost, long-lifetime instrumentation. While the ultimate success of this approach can only be determined by the passage of time, three factors have validated this approach in the short term:

- The much reduced development time and effort
- The changing of SBC processor boards during the development cycle, with different hardware configurations, with virtually no design effort
- The successful addition of a working prototype of an improved sensor platform

The reduced development time not only saved development costs, but also has improved reliability. The use of COTS equipment meant that the manufacturer, rather than the system designer, has performed the testing of the most complex components. The same applied to the operating system. This has resulted in a product many times more complex than the authors previous DSP based design, but which took a comparable amount of work to develop and, at this stage, has proven not only more reliable but also simpler to maintain.

The ability to rapidly adapt to different hardware platforms has been proven by the migration to an improved processor platform midway through the development cycle. This was performed with less than one hours work and required no modifications to the custom applications contained in the software suite subsystem. While this does not guarantee that all future modifications will be as straightforward, it does impart confidence in the approach.

As a result of work subsequent to this research project, an improved low-cost data acquisition circuit has been developed, reducing the noise level to approximately one half of that of the ADXL105 based circuit. The initial prototype of this circuit was integrated seamlessly into the CUSP Instrument. Further to this, an 18-bit data acquisition circuit, in the very early stages of development, has also been successfully integrated, but this process did require slight changes to the real-time data acquisition routine in the software suite subsystem. These two improvements offer the best proof

that the new approach allows rapid upward development by carefully choosing the interfaces to be scalable.

The second major component of this research was to determine the suitability of low-cost MEMs accelerometers for research grade seismological instrumentation. The sensors were determined to offer acceptable performance, however, the characterisation process presented in this thesis uncovers two key aspects not discussed by the manufacturer: zero-point thermal hysteresis and low frequency 1/f type noise. Fortunately, while neither of these aspects can be corrected for, they are not considered serious problems for strong motion analysis, as the hysteresis effect is noticeable only over very long periods after large temperature deviations, and the 1/f effect has a very small magnitude compared to strong motion records. The thermal offsets that are directly dependant on the temperature can be corrected for and the memory-efficient interpolated offset correction scheme works well. The axial misalignment is also measurable and is corrected for in real-time.

The final testing process, that of testing the CUSP Instrument on the shake table with genuine earthquake records, indicates that the system performs as well as expected. Comparison to the Kinemetrics Etna instrument and the shake table's reference accelerometer showed excellent agreement.

In general, the CUSP Instrument meets or exceeds all the design briefs requirements. The final costing of the completed instrument, including the case, the GPS receiver and even the manual, has been determined to cost less than just the populated and assembled core circuit board of the previous DSP based design.

The instrument has been successfully taken to commercial production, and some 10 instruments are in the field awaiting their first earthquake.

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Appendices

A Operation of PIC processor with variables of larger magnitude than native bus width

These code snippets illustrate the large numbers of cycles required to implement math routines with data variables larger than the bus width native to the processor. The first snippet combines the operations of a single multiply and accumulate instruction typical of a FIR filter implementation. This was compiled on the HITECH PICC c compiler with full optimisation and took 279 cycles per iteration of the loop.

```
long tmp = 1; // 32 bit temporary result of FFT multiplication

int data = 65534; // 16 bit data word

int tap = 12232; // 16 bit filter tap

long sum = 0; // 32 bit filter sum to produce final result

while (1==1)

{

    // 279 cycles per loop iteration

    sum = (data * tap) + sum; // result of data multiplied by tap

                                // operation added to the moving sum

                                // of filter

}
```

This second snippet performs the same operation but separates the MAC into a multiple and an acculturation instruction. This implementation too 287 cycles per iteration.

```
long tmp = 1; // 32 bit temporary result of FFT multiplication

int data = 65534; // 16 bit data word

int tap = 12232; // 16 bit filter tap

long sum = 0; // 32 bit filter sum to produce final result

while (1==1)

{

// 287 cycles per loop iteration

tmp = data * tap; // result of data multiplied by tap

sum = tmp + sum; // moving sum of filter

}
```